ORTEC
INCORPORATED
AN EG&G COMPANY

Model 455
Constant Fraction Timing
Single Channel Analyzer

Operating and Service Manual

ORTEC 455 CONSTANT FRACTION TIMING SINGLE CHANNEL ANALYZER

Manual Change Sheet

March 20, 1972
ECN 8

On Schematic 455-0101-S1, make the following changes:

Change the type designation for transistor Q28 from MPS6520 to MPS6531.

Change the type designation for transistors Q64 and Q65 from MPS3565 to MPS6531.

Change the value of capacitor C57 from 1 μF 35 V to 0.005 μF Disc.

Change the value of resistor R7 from 3.83 K to 4.22 K.

Change the value of resistor R150 from 100Ω to 47Ω.

8-8.71

ORTEC

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Printed in U.S.A.

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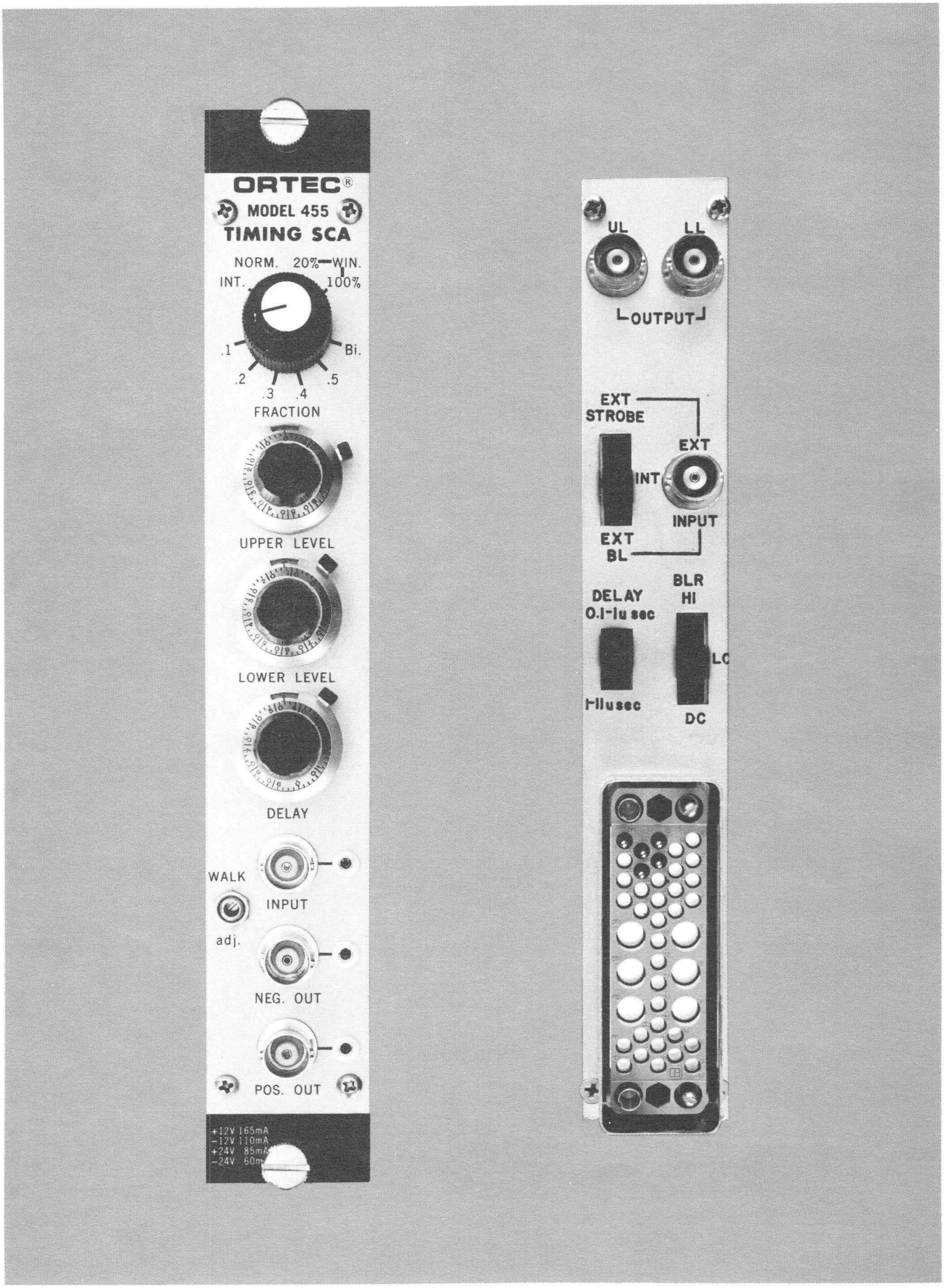

ORTEC®
MODEL 455
TIMING SCA
NORM.
20%
WIN.
INT.
100%
.1
.2
.3
.4
.5
Bi.
FRACTION
UPPER LEVEL
LOWER LEVEL
DELAY
WALK
adj.
INPUT
NEG. OUT
POS. OUT
+12V 165mA
-12V 110mA
+24V 85mA
-24V 60mA
UL
LL
OUTPUT
EXT
STROBE
EXT
INT
INPUT
EXT
BL
DELAY
0.1-1u sec
1-11u sec
BLR
HI
DC

ORTEC 455 CONSTANT FRACTION TIMING SCA

1. DESCRIPTION

The ORTEC 455 Constant Fraction Timing Single Channel Analyzer provides both pulse-height and timing analysis for unipolar and bipolar signals. The Constant Fraction Timing technique provides unexcelled timing on unipolar pulses and a unique crossover discriminator shows results better than heretofore possible with conventional leading edge or crossover discriminators.

Actual timing results obtained with the 455 and fast plastic scintillators are shown in Figure 1-1. The advantage of the constant fraction timing technique is readily apparent. With SCA's which utilize leading edge timing, the risetime of the input pulses causes degradation of time resolution because the pulses have varying amplitudes. Constant Fraction timing compensates for varying amplitudes and essentially eliminates this timing shift, giving consistently better timing results. For a 10% fraction, the output occurs soon after the peak of the input to facilitate gating and accumulation of data at very high input rates. This technique also minimizes timing shift and dead time when used with sodium iodide, silicon, and germanium detectors, thereby allowing better system time resolution and higher counting rates. Timing results paralleling those in Figure 1-1 are also possible with these detectors. The Constant Fraction technique makes it possible to realize significant improvements in most applications where analysis is made of the main amplifier output. It allows optimization of time resolution and extension of dynamic range for neutron-gamma discrimination.

The 455 can accurately analyze the output pulses of any shaping amplifier because the discriminator levels are extremely sharp and stable. A front-panel control selects four SCA modes: integral, 100%, 20%, and normal. These modes of operation are described in the specifications that follow.

With all of its versatility, ease of operation is an intrinsic quality of the 455. In all operating modes and with input pulse shaping from 0.1 to 10 μsec, no risetime compensation or other adjustments are necessary for proper operation.

The dc-coupled input of the 455 makes it possible to take full advantage of the baseline restoration of the main amplifier. For amplifiers with ac-coupled outputs, two ranges of dc restoration are available. These features ensure stable discrimination levels for widely varying input counting rates, and hence better energy discrimination.

The continuously adjustable output delay (two ranges covering 0.1 to 11 μsec) makes it possible to align output signals which have actual time differences without a need for additional delay devices or modules.

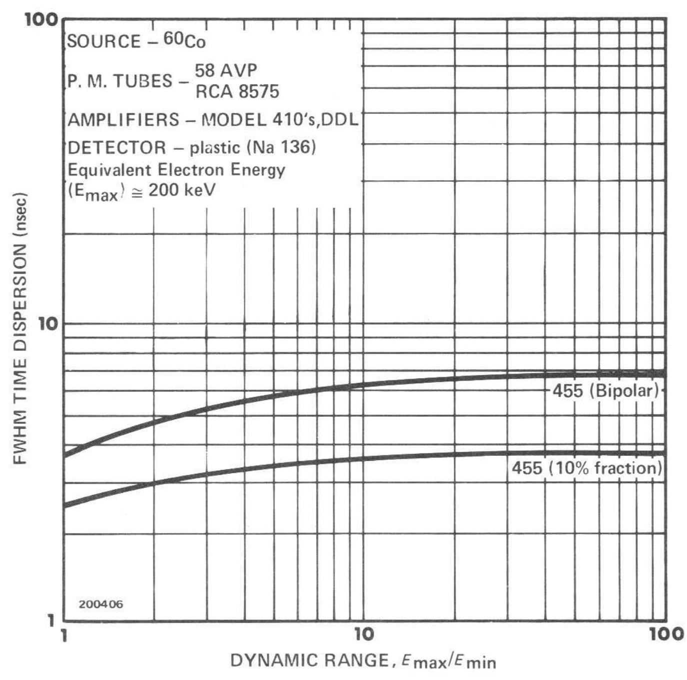


Figure 1-1. Time Resolution as a Function of Dynamic Range

2. SPECIFICATIONS

PERFORMANCE

Time shift vs pulse height (walk)

Constant Fraction Timing Mode

Walk (nsec) System A	Walk (nsec) System B	Dynamic Range
⩽± 1.5	⩽± 1.5	10:1
⩽± 3.7	⩽± 8	50:1
⩽± 4.5	⩽± 10	100:1

System A: Using ORTEC 410 Amplifier, single delay line mode, integrate ⩽ 0.1 μsec with delay lines of 0.2 to 2 μsec.

System B. Using ORTEC 450 or 451 Amplifier unipolar output with 0.5-μsec shaping time and 0.4 fraction.

Bi Mode

Walk (nsec)	Dynamic Range
⩽ ± 1	10:1
⩽ ± 2.5	50:1
⩽ ± 3	100:1

Using ORTEC 410 Amplifier, double delay line mode, integrate ⩽ 0.1 μsec with delay lines of 0.2 to 2 μsec.

Pulse pair resolution 0.5 μsec plus the delay time.

Nonlinearity Lower level ⩽ ± 0.25%, upper level ⩽ ± 0.25%. (Nonlinearity specifications are limited by the 10-turn potentiometer.)

Temperature stability
Upper level: ⩽ ± 0.005%/°C
Lower level: ⩽ ± 0.005%/°C
Delay: ⩽ ± 0.01%/°C

CONTROLS

LOWER LEVEL 10-turn control sets the lower level from 100 mV to 10 V (1000 divisions = 10 V).

UPPER LEVEL 10-turn control sets the upper level from 100 mV to 10 V (1000 divisions = 10 V).

DELAY RANGE Rear-panel switch selects range of 0.1 to 1.1 or 1.0 to 11 μsec delay.

DELAY 10-turn control for continuously adjusting output delay over selected delay range. In the external strobe mode the delay control adjusts the automatic reset time from ~ 5 to 50 μsec.

FRACTION A front panel switch selects the fraction of 0.1, 0.2, 0.3, 0.4, and 0.5 for Constant Fraction timing with unipolar or bipolar inputs, or Bi for zero crossing timing with bipolar inputs.

SCA MODES Front panel switch selects the following modes:

INTEGRAL Timing outputs occur for all signals with amplitudes above the lower-level discriminator setting.

NORMAL Timing outputs occur for signals with amplitudes between the lower-level and upper-level settings. The two controls are independently adjustable.

20% WINDOW Timing outputs occur for signals with amplitudes between the lower level and the sum of the lower-level and 0.2X upper level. The span (1000 divisions) of the upper-level control (window) is 2 V.

100% WINDOW Timing outputs occur for signals with amplitudes between the lower level and the sum of the lower level and the upper level. The span (1000 divisions) of the upper-level control (window) is 0 to 10 V.

RESTORER A 3-position rear-panel switch to allow input dc-coupling, or a high or low baseline restoration rate.

EXT STROBE/INT/EXT BASELINE A rear-panel switch selects internal strobe and baseline, external baseline reference, or external strobe. In the external baseline mode the lower level is set by the external reference. In the external strobe mode the timing outputs occur in coincidence with the strobe pulse.

WALK ADJUST Front panel screwdriver adjustment for precise setting of walk compensation.

CONNECTORS All signal connectors are BNC connectors (UG-1094/U).

INPUTS

Analog Input

Amplitude range 0 to 10 V

Pulse width range 0.2 to 20 μsec at half amplitude

Polarity Positive (unipolar) or positive portion leading (bipolar)

Input impedance 1000 ohms dc-coupled

External Input — Strobe/Baseline

Input impedance Greater than 1000 ohms dc-coupled

Strobe input +2 V min, +12 V max, 75 nsec min width

Baseline amplitude 0 to −10 V

OUTPUTS

Timing Outputs In the Constant Fraction mode the timing outputs occur when the input pulse has fallen from its peak by the selected fraction (plus the delay time). In the Bi (bipolar) mode the timing outputs occur when the input pulse crosses the baseline (plus the delay time).

NEG The current output produces 0.7 V minimum into 50 ohms with risetime < 5 nsec and width < 20 nsec (front panel).

POS Positive 5 V risetime less than 20 nsec, width 0.5 μsec, $Z_0 = < 10$ ohms (front panel).

Discriminator Outputs The signal occurs promptly when the input exceeds the discriminator threshold.

UL Positive 5 V, risetime < 20 nsec, width 0.5 μsec, $Z_0 = < 10$ ohms (rear panel).

LL Positive 5 V, risetime < 20 nsec, width 0.5 μsec, $Z_0 = < 10$ ohms (rear panel).

ORDERING INFORMATION

Power Required +24 V 70 mA +12 V 150 mA
−24 V 59 mA −12 V 100 mA

Weight (Shipping) 3 lb 6 oz (1.5 kg)

Weight (Net) 2 lb 7 oz (1.1 kg)

Dimensions Standard single width module per TID-20893 (Rev.)

3. INSTALLATION

3.1 General

The ORTEC 455 is designed for installation in an ORTEC 401A/402A Bin and Power Supply, which is intended for rack mounting. Any vacuum tube equipment operated in the same rack must be cooled by circulating air to prevent any localized heating of the all-transistor circuitry used throughout the 455. The temperature of equipment mounted in racks can easily exceed the recommended maximum of 120°F (50°C) unless precautions are taken.

3.2 Connection to Power

The 455 contains no internal power supply and so must obtain power from a Nuclear Standard Bin and Power Supply such as the ORTEC 401A/402A. Turn off the Bin power supply before inserting or removing modules. The ORTEC 400 Series modules are designed so that it is not possible to overload the Bin power supply with a full complement of modules in the Bin. Since this may not be true, however, when the Bin contains modules other than those of ORTEC design, check the power supply voltages after inserting modules. The 401A/402A has test points on the power supply control panel to monitor the dc voltages.

3.3 Connection to a Linear Amplifier

The input to the 455 is a front-panel BNC connector. It may be used to accept outputs from all linear amplifiers capable of producing 10-V unipolar or bipolar (positive lobe leading) signals onto a 1000-ohm load. The input operating range is from 100 mV to 10 V. If the amplifier output is attenuated so that it cannot exceed 10 V, the 455 may be used with vacuum tube amplifiers which are capable of output signals to 100 V. Simple resisitve attenuators installed in the vacuum tube amplifiers will make them compatible with related transistor equipment.

3.4 Linear Output Signal Connections and Terminating Impedance Considerations

The source impedance of the 0- to 10-V standard linear outputs of most ORTEC 400 Series modules is approximately 1 ohm. Interconnection of linear signals is thus not critical since the input impedance of the 455 is high and is not important in determining the actual signal span, 0 to 10 V, delivered into it. It is permissible to parallel several loads on a single output while preserving the 0- to 10-V signal span.

Short lengths of interconnecting cable (up to approximately 4 ft) need not be terminated. If, however, a linear signal is to pass through more than approximately 4 ft of cable, it should be terminated in a resistive load equal to the cable impedance. Since the output impedance is not purely resistive and is slightly different for each individual module, coaxial cable of more than 4 ft not terminated in the characteristic cable impedance will generally cause oscillations. These oscillations can be suppressed for any length of cable by terminating the cable properly, either in series at the sending end or in shunt at the receiving end of the line.

To terminate a cable properly at the receiving end, it may be necessary to choose an additional parallel resistance to the input resistance of the driven circuit to make the combination produce the desired termination resistance. Series terminating the cable at the sending end may be preferable when receiving-end terminating is not possible or desirable. Many ORTEC linear instruments include an alternate output connector for an output impedance of 93 ohms, and this connector may be used when 93-ohm cable is used for the interconnection; the impedance match will then be complete without any compensation at the high-impedance receiving end. When series terminating at the sending end, full signal span (amplitude) is obtained at the receiving end, only when it is essentially unloaded or is loaded with an impedance many times that of the cable. Since the input impedance of the 455 is 1000 ohms, a series termination at the sending end of the cable will normally provide satisfactory results.

BNC tee connectors and connectors with internal resistive terminators are available from a number of manufacturers in nominal values of 50, 100, and 1000 ohms to facilitate shunt termination at the receiving end of a cable. ORTEC stocks in limited quantity the following connector accessories for this application:

ORTEC C-27	100-ohm Resistive Terminator
ORTEC C-28	50-ohm Resistive Terminator
ORTEC C-29	BNC Tee Connector

4. OPERATING INSTRUCTIONS

4.1 Introduction to Fast Timing with Linear Signals

The precise determination of the time of a nuclear event, simultaneous with the measurement of its energy, has been restricted in the past to two timing techniques – zero crossing and level discrimination. In the zero-crossing method the timing SCA simply detects the time at which a bipolar linear signal crosses the baseline. For a double-delay-line shaped signal the zero-crossing phase point contains the same information as the 50% charge collection time on the leading edge of the signal. For some signals the zero-crossing point provides excellent time resolution.

There are two rather severe limitations to the zero-crossing technique. First, the amplitude noise of a bipolar signal is normally worse than a similarly shaped unipolar signal. Consequently, the edges of the energy window set by the SCA are not as precise as they would be for a unipolar signal. The second limitation of the zero-crossing technique is that the time information cannot be obtained until the signal crosses the baseline. The added time delay before getting the time information is not a severe limitation in DDL applications, but for simulated Gaussian-shaped signals the added delay may be several microseconds.

A simple level discriminator is used to obtain time information by the second technique. The usual mode of operation allows the level discriminator to trigger on the leading edge of the signal and to then reset when the signal falls below the discriminator level. Either of these trigger points can be used for the timing information. If the leading-edge trigger point is used, it must be delayed beyond the peak of the input signal for the single-channel amplitude decision to be made. The basic limitation of this system is that it introduces a time walk due to changing signal amplitudes, and the magnitude of the walk is usually equal to approximately the rise time of the signal. For different types of signals this walk will range from tens of nanoseconds to microseconds.

The 455 Constant Fraction Timing Single Channel Analyzer introduces a new timing technique that has been applied successfully in many fast timing applications. The CFPHT (Constant Fraction of Pulse Height Trigger) provides a degree of freedom from the major limitations imposed by the two techniques previously used. This feature can be understood best by observing the basic wave shapes in Figure 4-1. The linear signal is stretched and attenuated by an amount set by the fraction switch, F. The timing discriminator is triggered when the signal exceeds the lower-level discriminator. The timing discriminator is then reset when the signal becomes less than the stretched attenuated signal, as shown in Figure 4-1. For a signal with a different amplitude the stretched signal remains a constant fraction of the signal amplitude and the reset of the lower-level discriminator remains time-invariant. By selecting the fraction judiciously, an optimum time resolution for a given signal shape can be obtained, in addition to the systematic walk being eliminated. Bipolar inputs can be accepted but are not required. By selecting smaller fractions, the timing signal is derived very near the input signal peak to minimize the added delay before the signal arrives at the output.

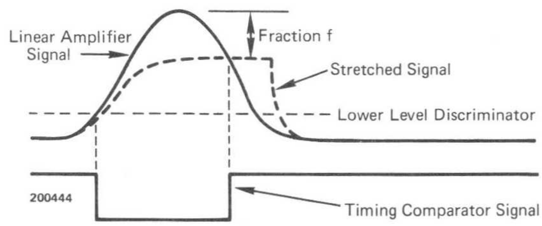


Figure 4-1. Principle of Constant Fraction Timing Signal Derivation

4.2 Typical Operating Conditions

Each application of the 455 involves a specific detector-to-amplifier configuration with unique pulse shape characteristics. Inspection of the details of the pulse will aid in selection of the timing fraction that will provide the best accuracy. The Constant Fraction is selected at a point along the decay of the input pulse and measured as a portion of the drop from peak amplitude toward the baseline. The optimum point along the decay is one with maximum slope and minimum noise; this will result in the largest slope-to-noise ratio. When two or more points offer about equal qualifications, the smaller fraction provides the earlier timing output.

Note that the fraction selected refers to the fraction of amplitude decay toward the baseline as measured from the input pulse peak. The settings are from 10% through 50%, plus Bipolar which is equivalent to a 100% fraction selection. The resulting stretched signal level is shown to be greater than the lower-level discriminator in Figure 4-1, but this condition is not required; in fact, the smaller amplitude input signals which are just large enough to trigger the lower-level discriminator will normally provide a stretched signal level below the lower level. See Sections 5.3 and 5.4 for further information.

4.3 Front-Panel Control Functions

Mode Selector. This four-position switch selects the integral mode or one of three circuits for the differential mode for the single-channel analyzer. For the integral mode the lower-level discriminator or an external baseline will determine response, and no upper-level discriminator is involved. For NORM, both discriminators are effective and their control ranges are completely independent; the Upper Level control must select a level greater than the Lower Level control or external baseline input, or no output can be generated. For the 20% WIN position, the Upper Level control selects the amount by which the upper-level discriminator reference exceeds the lower-level reference, and the control range is 0 to 2 V. For the 100% WIN position the same type of window circuit is effective, and the Upper Level control range is increased to the full 0- to 10-V dynamic range.

FRACTION. This six-position control is concentric with the mode selector. It permits selection of 10%, 20%, 30%, 40%, or 50% Fraction for timing or Bi, which is the conventional zero-crossing timing mode. See Sections 4.2, 5.3, and 5.4 for suggestions on the use of this switch.

UPPER LEVEL. This 10-turn precision potentiometer selects the upper-level reference. Its range is 0 to 10 V, read directly by the 1000 divisions of the duo-dial. When the 455 operates in its 20% Window mode, the effective range of the Upper Level control is 0 to 2 V.

LOWER LEVEL. This 10-turn precision potentiometer selects the lower-level reference, except when a rear-panel switch selects External Baseline. Its range is 0.1 to 10 V, read directly on the control.

DELAY. This 10-turn precision potentiometer adjusts the time from the timing comparator signal to the SCA output signals, except when a rear-panel switch is set at External Strobe. The delay can be adjusted from 0.1 through 11 μs; a rear-panel switch selects either an 0.1- to 1.1-μs range or a 1.0- to 11-μs range and the selected delay is read directly on the control of the potentiometer.

WALK ADJ. This screwdriver potentiometer adjusts for minimum time walk, as a fine control for any selected fraction. See Section 6.7 for further information.

4.4 Rear-Panel Control Functions

EXT STROBE/INT/EXT BL. This 3-position slide switch permits the adjacent BNC connector to be used for either of two externally controlled functions. When it is set at INT, neither of the external functions will be effective. When it is set at EXT STROBE, the SCA timing outputs occur in coincidence with an external strobe input pulse furnished through the BNC, and this must occur within less than 50 μs after the lower-level discriminator is triggered; the lower-level reference is set by the front-panel Lower Level control during the external strobe mode. When the switch is set at EXT BL, the front-panel Lower Level control is disconnected and the lower-level reference must be furnished by a 0- to negative 10-V bias through the adjacent BNC; internal strobe must be used, since there is no provision for an external strobe input.

DELAY. This slide switch selects either of the two effective ranges for the Delay front-panel control. The ranges are 0.1 through 1.1 μs and 1.0 through 11 μs.

BLR. This 3-position slide switch selects the input circuit appropriate to each specific application. The DC position is a dc-coupled input and may be used when there is no baseline offset furnished from the input pulse source. LO and HI positions refer to the average input pulse rate; the LO position selects a passive restoration circuit, while the HI position selects an active baseline restorer.

4.5 Connector Data

INPUT. A BNC connector accepts the analog input signals into an input impedance of 1000 ohms. The input circuit will be either dc- or ac-coupled, depending upon the selection of the rear-panel BLR switch. Either positive unipolar pulses or bipolar pulses with positive leading portion may be furnished within the 0- to +10-V linear range.

NEG. OUT. A standard ORTEC (and NIM) fast negative logic signal is available through this BNC connector for optimum timing resolution. This is a current output pulse that produces 0.7 V minimum into 50 ohms.

POS. OUT. A standard ORTEC (and NIM) slow positive logic signal is available through this BNC connector for applications such as analyzer gating and coincidence timing.

UL. A standard ORTEC (and NIM) slow positive logic signal is furnished through this BNC connector each time the upper-level discriminator is triggered, without regard to the internal use of the upper-level response.

LL. A standard ORTEC (and NIM) slow positive logic signal is furnished through this BNC connector each time the lower-level discriminator is triggered, without regard to the internal use of the lower-level response.

EXT INPUT. This BNC connector accepts either external strobe pulses or an external baseline bias level, depending upon the selection of the adjacent 3-position slide switch.

Test Points. Oscilloscope test points for monitoring the input and the two single-channel outputs on the front panel are available at each connector. Each test point is connected to its respective connector through a 470-ohm series resistor.

5. CIRCUIT DESCRIPTION

5.1 Input Circuit

The input signal is presented to a dc-restorer circuit, or is dc-coupled, directly into a unity gain amplifier, Q5 to Q9. A rear-panel switch selects either HI or LO dc-restoration rate or dc-coupling. Input capacitor C1 is simply bypassed for dc-coupling. For the LO restoration rate, Q1 and Q2 form a Robinson type of restorer circuit. For the HI restoration rate, Q3 and Q4 operate as a high-gain differential amplifier to feed back a voltage to the emitter of Q2 that is inversely proportional to the dc offset voltage at C1. Thus, in the HI rate circuit, restoration of the voltage to zero is achieved by an active closed-loop feedback amplifier.

Following the restorer, the signal is attenuated for half of its input value, using resistors R9 and R10. It is then buffered by the unity gain amplifier, Q5 – Q9, and furnished to four internal circuits. The amplifier is dc-coupled with a very low output impedance to drive all three comparators, IC 5 through IC 7, with no appreciable loading effects due to the comparator base currents. The signal at the unity gain amplifier output has half of the input amplitude for its positive polarity; any negative polarity included in the input is clipped two diode junctions (approximately -1.4 V) below zero. The quiescent voltage at the amplifier output is zero volts.

The amplifier output signal is presented to three voltage comparators, IC 5, IC 6, and IC 7, and to a pulse stretcher, Q17 through Q21. Comparators IC 5 and IC 6 form a conventional single-channel pulse-height analyzer. Comparator IC 7 and the stretcher perform a unique timing analysis.

5.2 Single Channel Analyzer

Lower Level comparator IC 6 accepts a bias level B from IC 8B and the unity gain amplifier output. In the quiescent state, IC 6 output is $\simeq$ +1.5 V. When the signal level exceeds the reference level B, the output switches rapidly to $\sim$ -0.5 V and remains until the signal level drops below the reference level again. The comparator is a type μA710 with fast switching speed, and responds to signals as short as 200 ns. The negative transition of the output triggers two monostables; one forms a Lower Level output pulse through the rear-panel LL connector and the other is a temporary memory to hold the response until an output trigger occurs.

Upper Level comparator IC 5 accepts a bias level A from IC 8A and the output from the unity gain amplifier. Its operation is identical to that of IC 6, discussed above, and this comparator also triggers two monostables; one forms an Upper Level output pulse and the other is a temporary memory.

The Lower Level output pulse is a NIM standard slow positive pulse formed when IC 4B and Q32 and Q33, a monostable, receives the negative transistion of the IC 6 comparator output. The output pulse duration is 0.5 μs and its amplitude is +5 V approximately. The pulse occurs on the leading edge of the input pulse when the input exceeds the Lower Level bias and is available through the rear-panel LL connector.

The Upper Level output pulse is identical to the Lower Level output discussed above and is generated by IC 4A, Q40, and Q41. It occurs on the leading edge of the input pulse when the input exceeds the Upper Level bias and is available through the rear-panel UL connector.

The temporary memory for the Lower Level comparator is IC 2, sections A, B, C, and D. It is a monostable with a duration of 50 μs but is normally reset prior to this time, just after the pulse-height decision is made. Its output goes from +1.5 V to -0.5 V and is furnished as one of two inputs to IC 1D. The temporary memory for the Upper Level comparator is IC 1, sections A, B, and C. It also has a duration of 50 μs, subject to prior reset. The output from this memory, furnished as the second input to IC 1D, goes from -0.5 V to +1.5 V when it is triggered.

When either input (or both) to OR gate IC 1D is at +1.5 V, it will drive Q67 into saturation, thus preventing the timing signal from appearing at the collector of Q38. A single-channel output pulse will be generated by a delay monostable, Q45 to Q49, when it recovers after being triggered by a pulse through Q38; but Q67 must be cut off to permit the trigger pulse to reach the monostable. Only when both IC 1D gate inputs are at the low state ($\sim$ 0 V) will the trigger pulse be effective. This condition is equivalent to the logic that permits the generation of a single-channel output pulse and allows the timing circuit to determine when the pulse will be generated. The signal into IC 1D from IC 1A, B, and C is low when the Upper Level discriminator has not been triggered or when the front-panel selector switch is set for Integral mode operation. The signal into IC 1D from IC 2 is low only after the Lower Level discriminator has been triggered. Thus, for the Integral mode of operation, a single-channel output will be generated for each pulse that has an amplitude greater than the setting of the Lower Level bias B. For Normal and Window modes a single-channel output will be generated if the input pulse amplitude exceeds the B reference level but does not exceed the A reference level (Upper Level). For each such input pulse with too large an amplitude, a permissive condition will exist for a short time interval during the input pulse rise time, but the output trigger will not occur until a selected time after the input pulse peak; so the false indication will not be sampled.

5.3 Reference Levels

A 3-position rear-panel switch selects External Strobe with internal baseline control, External Baseline control with internal strobe, or Internal strobe and baseline. The BL switch position selects external baseline control, which removes the Lower Level control from the 455 internal circuit and allows a 0- to –10-V signal to be accepted through the rear-panel BNC connector for use as the B reference level after attenuation by a factor of 2. For either of the other two switch positions, reference level B is determined by the setting of the front-panel Lower Level control.

The Lower and Upper Level channels have a common -5-V reference level, regulated by D8. Lower Level adjustment R39 selects a level between 0 and -5 V and applies it to unity gain amplifier Q56, Q59, Q60, Q61, and Q65. The unity gain amplifier has a high input impedance for minimum current drain from the D8 reference source and for buffering the potentiometer from all other circuitry. Upper Level adjustment R29 independently selects a level between 0 and -5 V and applies it to its unity gain amplifier, Q54 through Q57 and Q67.

Following the unity gain amplifiers is the dual operational amplifier IC 8. The unity gain amplifier for the Lower Level furnishes its output directly to IC 8B to be inverted for a 0- to +5-V reference level B. The input to IC 8A is determined by the setting of the front-panel mode selector and either is the independent Upper Level selection or is the sum of the Lower Level and the Upper Level adjustments. Its output is reference level A, applied to the Upper Level comparator.

For the Integral mode the Upper Level reference A is full-range 0 to +5 V. The Upper Level comparator triggers its monostables in the normal manner to provide an Upper Level output signal if the input amplitude exceeds reference level A; the mode switch furnishes ground potential to OR gate IC 1D to overcome and defeat any inhibit that is generated in IC 1A, B, and C.

For the Normal mode the same circuit is used for the input to the Upper Level comparator, and the mode switch now opens the ground circuit and permits the response in the Upper Level to inhibit a single-channel output pulse.

For the 20% Window mode, reference B is determined by the setting of the Lower Level adjustment or by the External Baseline input and is also applied through R61 into IC 8A. The signal from the Upper Level adjustment is applied through R62 and is summed with the signal from the Lower Level adjustment at the input to IC 8A. Thus the reference level A is based on both adjustment levels, and the range of the Upper Level (Window) above the Lower Level is 20% of the normal full range.

In the 100% Window mode a similar circuit connects the Upper Level selection into the summed junction through R60; so it is not attenuated and the range is 100% of the normal full range.

5.4 Internal Timing Signal

A timing signal is derived with two basic circuits, pulse stretcher Q17 through Q29 and fast comparator IC 7. The pulse stretcher accepts an attenuated signal from the unity gain amplifier, Q5 through Q9. Attenuation is selected by the setting of the FRACTION switch on the front panel. The attenuated positive portion of the signal passes through the stretcher amplifier, Q17 to Q21, which charges C49 through D16 until the input signal peak occurs. This charge is maintained by the Q23 stretcher gate, opened at the proper time. The timing reference for comparator IC 7 is obtained from the charge on C49 through unity gain amplifier Q24 through Q29.

During quiescent intervals the B reference level is applied as the timing reference input through Q15 and Q16. When the input pulse amplitude exceeds the B reference level, comparator IC 7 switches from high to low. This coincides with the switching time of IC 2, which switches Q11 off and Q12 on. From this time until internal reset, the timing reference level is the stretched output through Q13 and Q14 and the input signal will logically exceed the timing reference level until it reaches a point on the decay of the input signal where there is a crossover. At the time that the input signal crosses through the timing reference level IC 7 resets for a high output, this transition being the timing signal. IC 7 remains in its high state only momentarily if the input signal exceeds the B reference level. After the signal decreases below the B reference level, IC 7 again switches to high and this closes the stretcher gate to discharge C49.

The timing signal from IC 7 is differentiated and inverted by C56, Q34, and Q44 and is routed to parallel gate Q38 and Q67. If the input signal has met the single-channel logic conditions, the gate will be opened and the timing signal triggers the delay generator, Q45 and Q46.

5.5 Single Channel Output

The delay generator, Q45 and Q46, is a monostable with an adjusted recovery period. The delay interval is selected within the range of 0.1 through 11 μs with front-panel controls. The delay generator output triggers a current switch, Q50 to Q53, to produce the NIM standard Fast Negative output, and it also triggers a 0.5-μs shaping monostable, IC 4C, Q42, and Q43 for the NIM standard Slow Positive output.

5.6 External Strobe Operation

The External Strobe mode can be selected by setting the rear-panel switch at its STROBE position. A NIM standard Slow Positive signal through the rear-panel BNC connector will then determine when the output pulse will be generated. For this mode of operation all of the internal logic operates in the same manner as for internal strobe, except that the delay time of monostable Q45 and Q46 is extended and the external strobe will reset it prior to its natural recovery to generate the output. The delay circuit recovery is extended to ~ 50 μs by setting the front-panel controls for maximum delay, 11 μs.

6. MAINTENANCE INSTRUCTIONS

6.1 Testing Performance

6.1.1 Introduction. The following material will aid in installing and checking out the 455. It consists of information on front panel controls, waveforms, test points, and output connectors.

6.1.2 Test Equipment. The following, or equivalent, test equipment is needed:

1. ORTEC 419 Pulse Generator
2. Tektronix 454 Series Oscilloscope
3. 100-ohm BNC terminators
4. ORTEC 410 or 450 Amplifier
5. Schematics and Block Diagrams for the 455 Timing Single Channel Analyzer

6.1.3 Preliminary Procedures.

1. Visually check module for possible damage due to shipment.
2. Plug module into Nuclear Standard Bin and Power Supply, e.g., ORTEC 401A/402A, and check for proper mechanical alignment.
3. Connect ac power to Bin.
4. Switch on ac power and check the dc power voltages at the test points on the 402A Power Supply control panel.

6.1.4 Testing the Single Channel Function

1. Connect the direct output of the pulse generator to the scope trigger. Connect the attenuated output of the pulse generator to the input of the Amplifier. Place all attenuator switches on the pulse generator to the OUT position except one switch, which should be a X10 switch. Adjust the pulse generator output and/or amplifier gain control to achieve an amplifier output pulse height of approximately 10 V.

2. Connect the amplifier output to the 455 input. Set the 455 mode selector at INT. Set the rear-panel 3-position slide switch at INT and the BLR switch at DC. Adjust the Lower Level dial to 500/1000 divisions. There should now be an output from both the NEG and POS OUT connectors on the 455. Turn the Lower Level control to read 1000, then adjust the pulse height from the amplifier so the 455 half-triggers. Now set the X2 attenuator switch on the pulse generator to reduce the pulse amplitude to half of the previous level. Reduce the 455 Lower Level control; the half-trigger point should occur at ~ 500 dial divisions. Next, reduce the Lower Level control to 400 dial divisions and set the mode selector at 100% WIN. Starting with the Upper Level control well above 100 dial divisions, reduce the Upper Level toward zero; a half-trigger point should be noted at about 100 dial divisions. Now switch the mode selector for a 20% WIN setting, and advance the Upper Level control until the 455 again half-triggers, which should occur with the control at about 500 dial divisions. These steps will prove that the 455 is operating correctly as a single-channel analyzer in all three basic modes. The steps may be repeated for other levels of pulse height and for other logical combinations of Lower Level and Upper Level adjustments and for the NORM mode selection.

6.2 Calibration Adjustments

6.2.1 Input Offset Adjustment. Potentiometer R12 is used to zero the dc offset at the amplifier input. R12 is the 4th potentiometer from the front of the printed circuit board. Use TP4 to observe the dc offset. TP4 is the 2nd test point from the front panel near the top of the printed circuit board. With no input signal applied, set R12 for zero ∓2 mV at TP4.

6.2.2 Lower Level Zero Adjustment. Potentiometer R52 adjusts the Lower Level Zero, and is the 2nd from the front of the printed circuit board. Use the following steps:

1. Connect the system shown in Figure 6-1.
2. Set the 455 for BLR LO, for the INT mode, and for a Lower Level setting of 1000 dial divisions. Adjust the pulser for half-triggering, which should occur at about 10 V.
3. Reduce the Lower Level control to 10 dial divisions and attenuate the pulser output by 100; this should provide 100 mV to the 455 input. Adjust R52 for half-triggering of the Lower Level output.
4. Repeat steps 2 and 3 to overcome any interaction of controls.

6.2.3 Upper Level Zero Adjust. Zero adjustment for the Upper Level controls uses R57, which is the 3rd potentiometer from the front panel on the printed circuit board. Use the four steps of Section 6.2.2 with the 455 set for NORM mode. Observe the output through the UL connector on the rear panel.

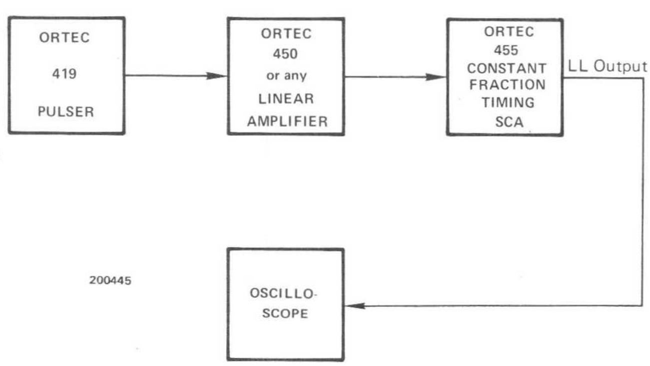


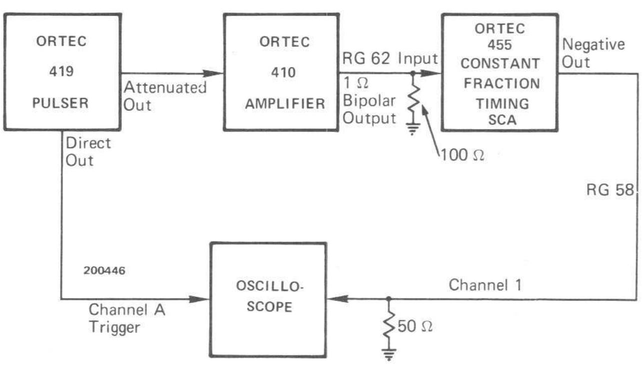
Figure 6-1. Basic Interconnections for Level Calibrations

6.2.4 Timing Discriminator Sensitivity Adjustments. The timing discriminator should trigger at an amplitude only slightly less on the input signal than the Lower Level trigger. After the Lower Level has been adjusted as discussed in Section 6.2.2, connect a sensitive dc millivoltmeter to pin 2 of IC 7. Adjust R100, at the front on the printed circuit board, for 20 to 30 mV on the meter.

6.3 Testing the 455 Timing Walk

A system for checking the walk of the 455 SCA output is shown in Figure 6-2. Adjust the pulser's Normalize control for 10 V at the 455 input. Set the Tektronix 454 Oscilloscope B Sweep Mode to B Starts After Delay Time; set the Horizontal Display switch to B (Delayed Sweep); set the Delay Time to 0.2 μs and X10 Magnified, for 5 ns/division; adjust the Delay Time Multiplier control until the negative signal appears at the center of the oscilloscope face. The intensity should be near maximum.

1. Set a X10 attenuation in the 419 for a 1-V input to the 455. Adjust the front-panel WALK ADJ for zero walk with X10 attenuation. Observe the walk for X2 and X5 attenuation.
2. Set a X50 attenuation in the 419 for a 200-mV input to the 455. Readjust the front-panel control if necessary for a zero time shift for the X50 attenuation. Observe the time shift for X5, X10, and X20 attenuation.



Oscilloscope Settings:	Fine Gain — minimum Coarse Gain — 1 Input Attenuator — X1
410 Amplifier Settings:	Diff control — Double Delay Line Integrate — Out Input Polarity — Pos
419 Pulser Settings:	X10 Attenuation — In Polarity — + (Positive)
455 Settings:	Lower Level — 10/1000 Mode — INT (Integral) Ext/Int/Strobe — INT (Internal) Delay — minimum BLR — DC

Figure 6-2. System Interconnections for 455 Walk Test

3. Set a X100 attenuation in the 419 for a 100-mV input to the 455. Adjust the front-panel WALK ADJ control for zero time shift for X100 attenuation. Observe the time shift for X5, X10, X20, and X50 attenuation. Note that the noise of the 410 Amplifier begins to dominate at the X100 attenuation level, causing a time dispersion which makes the time centroid difficult to locate. The dispersion will normally be approximately 4 ns.

6.4 Procedure for Adjusting Walk

The ORTEC 455 Constant-Fraction Discriminator is adjusted for minimum walk at the factory for the 10% fraction on unipolar signals. The Walk adj. control on the front panel adjusts the dc level of the stretched signal as shown in Figure 6.3.

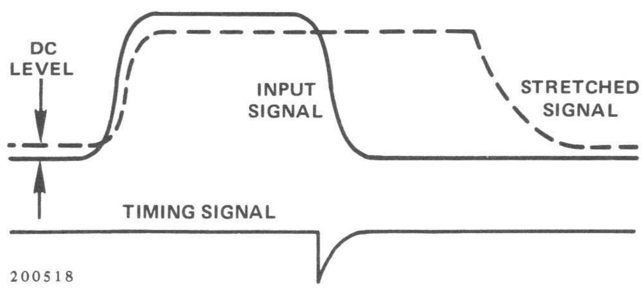


Figure 6.3. Waveforms for Proper Adjustment

For small input signals, the timing signal will occur on the leading edge of the input signal if the Walk adj. control is set too far counterclockwise. This malfunction is shown in Figure 6.4.

The condition in Figure 6.4 can be observed by triggering the oscilloscope from the pulse generator and observing either the positive or negative output on the oscilloscope. For 10%-fraction mode and a 200-mV input signal, turn the Walk adj. clockwise until the output jumps from left (Figure 6.4) to right (Figure 6.3). Do not operate the leading edge mode as shown in Figure 6.4.

Since the 455 is dc-coupled, a small dc offset at the input can cause the apparent malfunction shown in Figure 6.4. If the user does not desire to ensure that the amplifier providing the 455 input signal is dc zeroed, he should always use the dc-restoration mode on the 455.

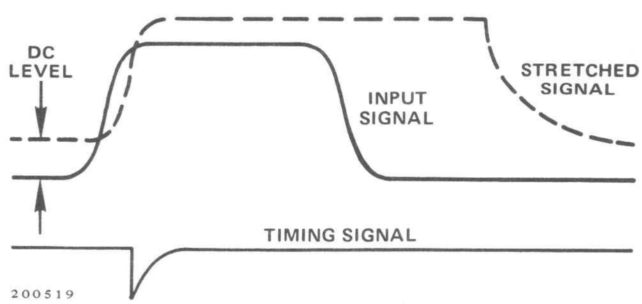


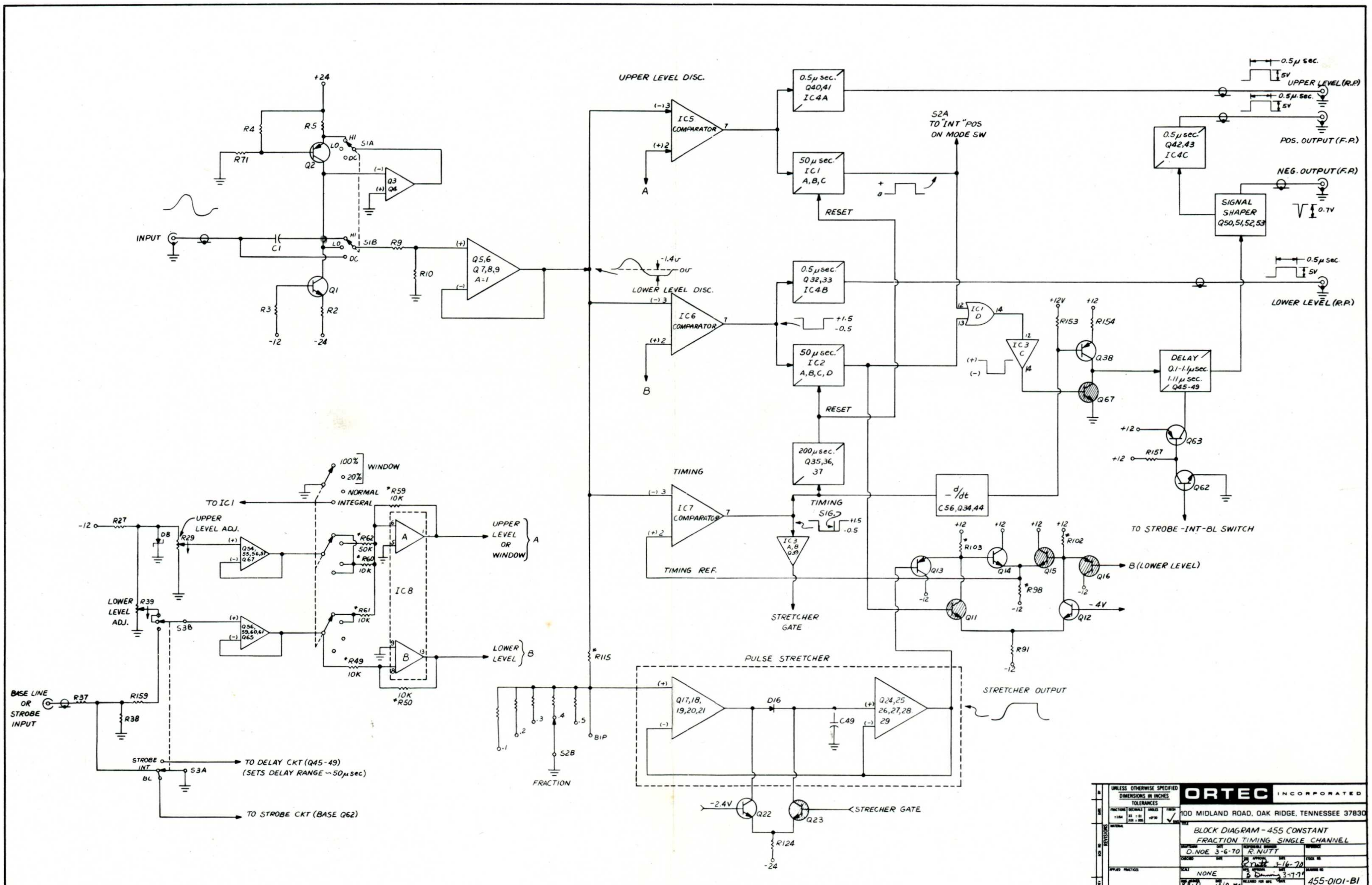
Figure 6.4. Waveforms for Improper Adjustment

BIN/MODULE CONNECTOR PIN ASSIGNMENTS FOR AEC STANDARD NUCLEAR INSTRUMENT MODULES PER TID-20893

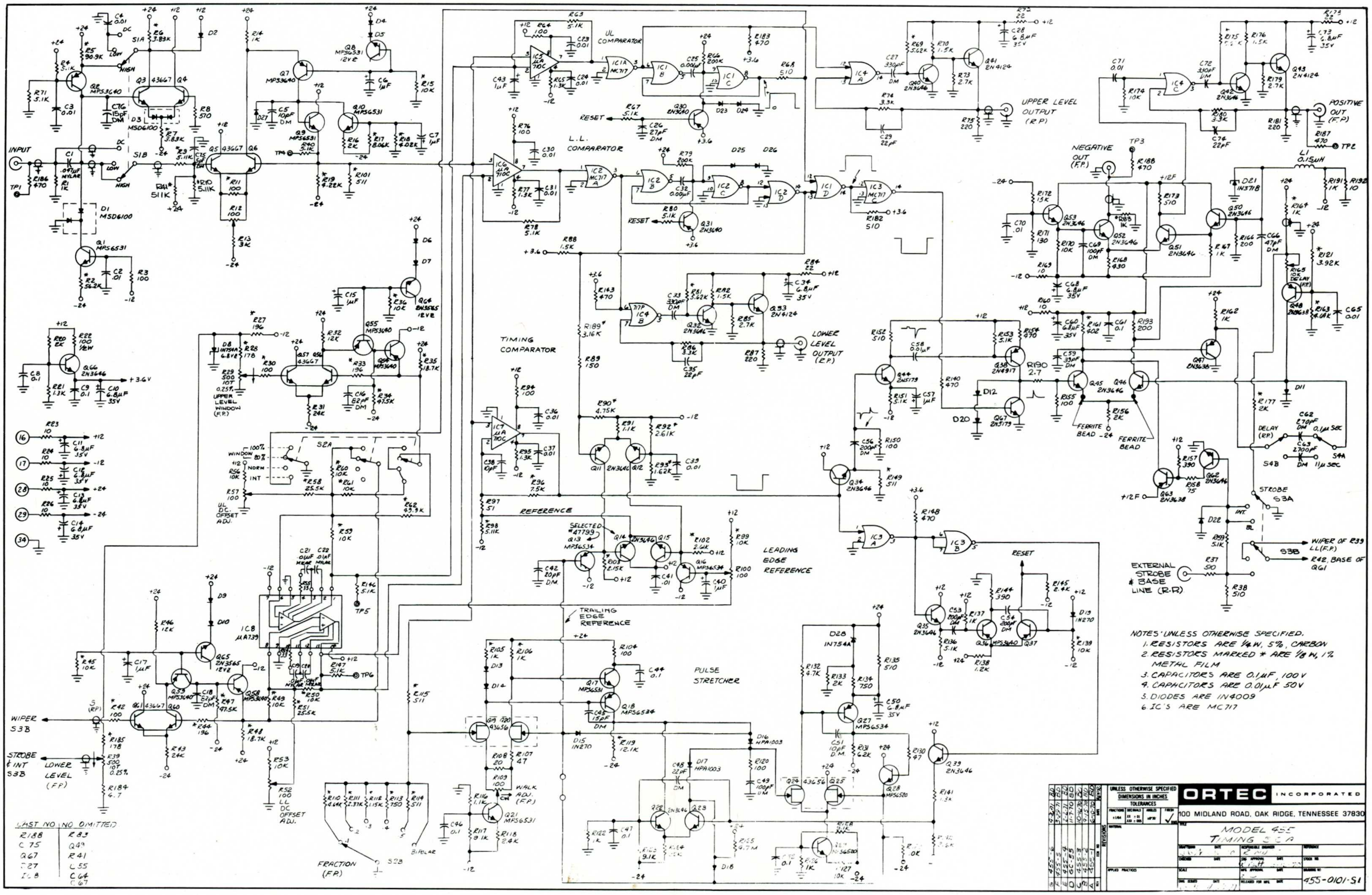
Pin	Function	Pin	Function
1	+3 volts	23	Reserved
2	-3 volts	24	Reserved
3	Spare Bus	25	Reserved
4	Reserved Bus	26	Spare
5	Coaxial	27	Spare
6	Coaxial	*28	+24 volts
7	Coaxial	*29	-24 volts
8	200 volts dc	30	Spare Bus
9	Spare	31	Spare
*10	+6 volts	32	Spare
*11	-6 volts	*33	115 volts ac (Hot)
12	Reserved Bus	*34	Power Return Ground
13	Spare	35	Reset
14	Spare	36	Gate
15	Reserved	37	Spare
*16	+12 volts	38	Coaxial
*17	-12 volts	39	Coaxial
18	Spare Bus	40	Coaxial
19	Reserved Bus	*41	115 volts ac (Neut.)
20	Spare	*42	High Quality Ground
21	Spare	G	Ground Guide Pin
22	Reserved		

**These pins are installed and wired in parallel in the ORTEC 401A and 401B Modular System Bins.*

The transistor types installed in your instrument may differ from those shown in the schematic diagram. In such cases, necessary replacements can be made with either the type shown in the diagram or the type actually used in the instrument.


UPPER LEVEL DISC.
IC5 COMPARATOR
0.5μ sec. Q40,41 IC4A
50μ sec. IC1 A,B,C
RESET
S2A TO "INT" POS ON MODE SW
UPPER LEVEL (R.P.)
POS. OUTPUT (F.P.)
0.5μ sec. Q42,43 IC4C
NEG. OUTPUT (F.P.)
SIGNAL SHAPER Q50,51,52,53
LOWER LEVEL (R.P.)
INPUT
Q5,6 Q7,8,9 A=1
LOWER LEVEL DISC.
IC6 COMPARATOR
0.5μsec. Q32,33 IC4B
50μ sec. IC2 A,B,C,D
DELAY 0.1-1.1μsec 1.11μ sec. Q45-49
TIMING
IC7 COMPARATOR
200μ sec. Q35,36,37
-d/dt C56,Q34,44
TO STROBE-INT-BL SWITCH
WINDOW
NORMAL
INTEGRAL
TO IC1
UPPER LEVEL ADJ.
LOWER LEVEL ADJ.
IC8
UPPER LEVEL OR WINDOW
LOWER LEVEL
TIMING REF.
STRETCHER GATE
B (LOWER LEVEL)
BASE LINE OR STROBE INPUT
TO DELAY CKT (Q45-49) (SETS DELAY RANGE -50μ sec)
TO STROBE CKT (BASE Q62)
FRACTION
PULSE STRETCHER
STRETCHER OUTPUT
STRECHER GATE
ORTEC INCORPORATED
100 MIDLAND ROAD, OAK RIDGE, TENNESSEE 37830
BLOCK DIAGRAM - 455 CONSTANT FRACTION TIMING SINGLE CHANNEL
D. NOE 3-6-70
R. NUTT
455-0101-B1

The transistor types installed in your instrument may differ from those shown in the schematic diagram. In such cases, necessary replacements can be made with either the type shown in the diagram or the type actually used in the instrument.


INPUT
UL COMPARATOR
L.L. COMPARATOR
UPPER LEVEL OUTPUT (R.P.)
NEGATIVE OUT (F.P.)
POSITIVE OUT (F.P.)
LOWER LEVEL OUTPUT (F.P.)
TIMING COMPARATOR
UPPER LEVEL WINDOW (F.P.)
U.L. DC OFFSET ADJ.
REFERENCE
LEADING EDGE REFERENCE
TRAILING EDGE REFERENCE
PULSE STRETCHER
WALK ADJ. (F.P.)
FRACTION (F.P.)
BIPOLAR
LOWER LEVEL (F.P.)
L.L DC OFFSET ADJ.
WIPER S3B
STROBE & INT S3B
DELAY (R.P.)
STROBE S3A
WIPER OF R39 LL(F.P.)
R42, BASE OF Q61
EXTERNAL STROBE & BASE LINE (R.P.)
FERRITE BEAD
RESET
LAST NO. | NO. OMITTED
R188 | R83
C75 | Q49
Q67 | R41
D27 | C55
IC8 | C64
C67
NOTES: UNLESS OTHERWISE SPECIFIED.
1. RESISTORS ARE 1/4 W, 5%, CARBON
2. RESISTORS MARKED * ARE 1/8 W, 1% METAL FILM
3. CAPACITORS ARE 0.1μF, 100V
4. CAPACITORS ARE 0.01μF 50V
5. DIODES ARE IN4009
6. IC'S ARE MC717
UNLESS OTHERWISE SPECIFIED
DIMENSIONS IN INCHES
TOLERANCES
ORTEC INCORPORATED
100 MIDLAND ROAD, OAK RIDGE, TENNESSEE 37830
MODEL 455
TIMING SCA
455-0101-S1

Model 455 Constant Fraction Timing SCA
Operating and Service Manual

For more information on ORTEC products or their applications, contact your local ORTEC representative or:

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United Kingdom: ORTEC Limited, Dallow Road, Luton, Bedfordshire, England, Telephone LUton 27557, Telex 82477

Other: ORTEC Incorporated, 100 Midland Road, Oak Ridge, Tennessee 37830, Telephone (615) 482-4411, TWX 810-572-1078, Telex 055-7450

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