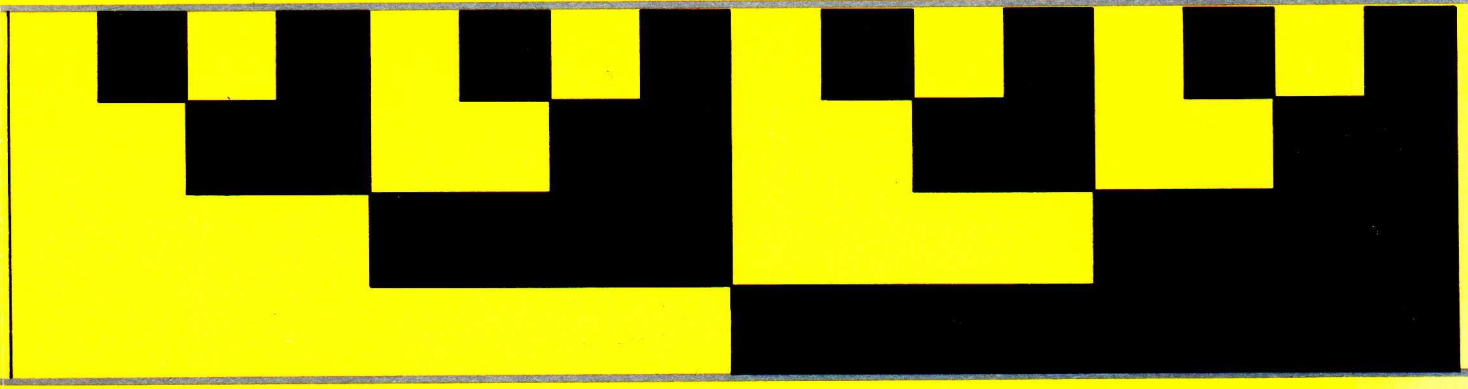
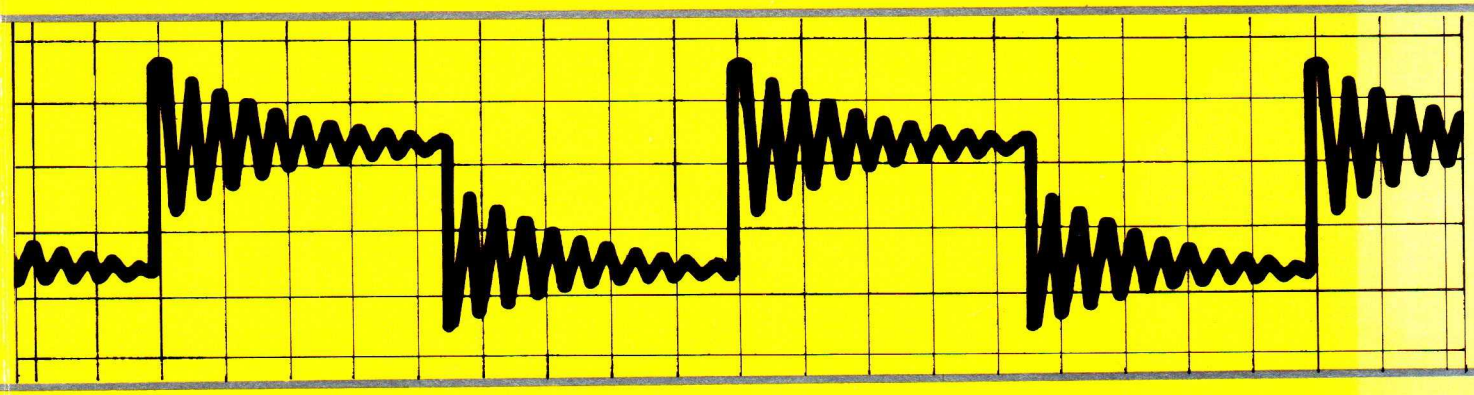
PHILIPS

digital exercises

APPLIED MEASUREMENTS IN DIGITAL AND PULSE TECHNIQUE





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DIGITAL EXERCISES

Applied measurements in digital and pulse technique

This book is based on the original work by
civ.ing. Tommy Kjellander of the Royal Institute of Technology, Stockholm, Sweden

Contents

Foreword

The intention with these digital exercises is primarily to give the teacher, in the time tabled education, access to thoroughly worked out exercises in digital technique.

The exercises are written in such a way that they preferably can be used also for home studies. The book starts with measurements of fundamental pulse parameters and estimations of the oscilloscope influence on the measuring result. After that, there is a row of exercises intended to create a good understanding of TTL and MOS logic. The differences between these logics are the subject of some exercises.

A few more demanding exercises are included to stimulate the student to further, own developments.

Each exercise starts with a list of equipment used and a short explanation of the objective. The measuring results are verified by means of photographs taken from the oscilloscope screen.

As well as this book gives a good training in digital technique, it also demands preinformation to the student. Basic theoretical knowledge of pulse and digital technique is essential for a good understanding of the exercises.

A suitable introduction to basic binary theory and logic circuits is Philips Digital Instrument Course, Part I, by A. J. Bouwens.


PM 5704 pulse generator 0.1 Hz - 10 MHz
MADE IN SWEDEN
PHILIPS
REPETITION TIME
X
DURATION
X
SINGLE SHOT
SQUARE WAVE
TTL PULSE OUT
DC OUTPUT
+5 V
MAX 1.5 A
POWER
ON
OFF
TRIGG. / GATE IN
>+1V
NORMAL
COMPLEMENT

Pulse Generator Principles

The block diagram figure 2.1 shows the most important stages of the pulse generators PM 5704 and PM 5705.

Astable multivibrator
The astable multivibrator generates square wave pulses from which all internal pulses are derived. Switch SK1, REP.TIME, and its vernier, R1, enable adjustment of the repetition time between 10 s and 100 ns.

The multivibrator is inoperative when switch SK1 is set to position EXT+ or EXT—.

Trigger circuit
In the EXT+ and the EXT— modes the generator can be triggered by the positive or negative slope of an external signal, applied at connector TRIGG/GATE IN, BU1.

The triggering signal is fed to a Schmitt trigger, producing an appropriate signal for the remaining circuits of the generator. With no triggering signal applied, a single pulse is generated by the Schmitt trigger when push-button SK3, SINGLE SHOT, is depressed. With switch REPETITION TIME set to one of the time positions, the astable multivibrator can be gated by a signal applied at input TRIGG/GATE IN. Bursts of pulses which are synchronized with the gating signal are then obtained.

Duration circuit, TTL amplifiers and switch SQUARE WAVE
The duration circuit produces pulses whose duration is set with the DURATION control, SK2, and its vernier R2. When the SQUARE WAVE switch SK4 is released the output from the duration circuit is fed to the two TTL amplifiers providing TTL outputs with variable duration. When the SQUARE WAVE switch is depressed the duration circuit is disconnected from the TTL amplifiers. The signal produced by the internal multivibrator ,or the Schmitt trigger, is fed directly to the TTL amplifiers.

In the PM 5705 the PULSE OUT output, however, still provides the signal with variable duration. In the EXT+ or EXT— positions of switch REPETITION TIME and with switch SQUARE WAVE depressed a triggering signal applied at TRIGG/GATE in determines the TTL pulse duration. When the REPETITION TIME switch is set to one of the time positions and no triggering signal is applied at TRIGG/GATE IN, the TTL OUT is a fixed square wave.

Output stage, baseline offset
In the PM 5705, the pulses, normal or complementary, are fed from pushbutton switch SK6, COMPL. via a driver stage to the output amplifier in which the pulse amplitude can be continuously set with AMPLITUDE control R3.
Control BASELINE OFFSET, R4, controls a clipping-diode in the baseline stage thus providing a baseline shift.

The setting of the BASELINE OFFSET control does not influence the pulse top. The sum of baseline voltage and the pulse amplitude is equal to the preset pulse amplitude.

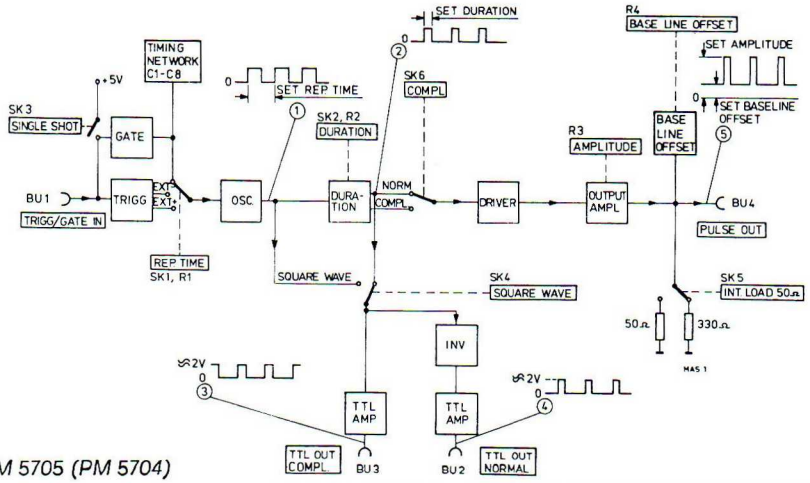
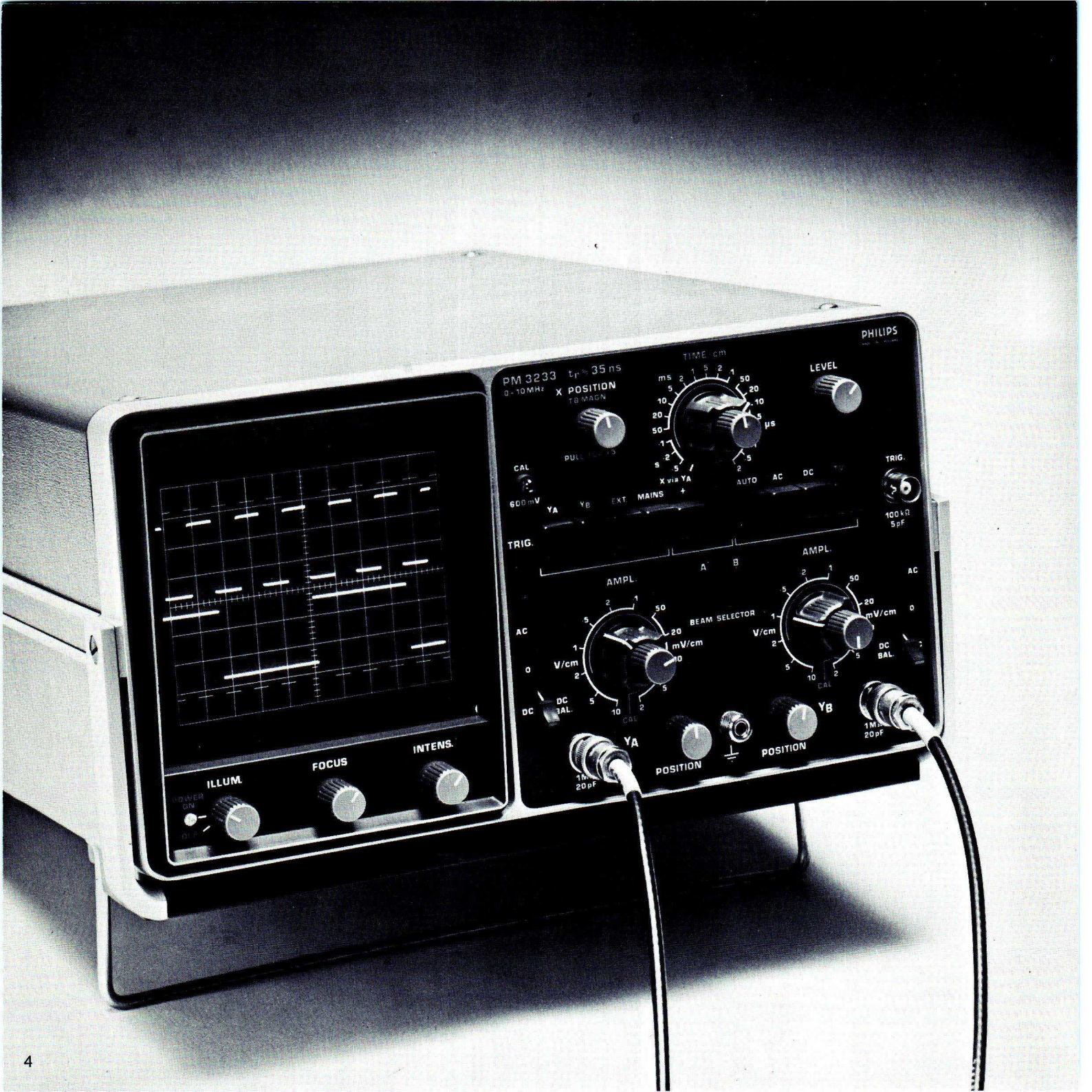


Fig. 2.1. Block diagram PM 5705 (PM 5704)


PHILIPS
PM 3233
0-10MHz
X POSITION
TIME/cm
LEVEL
CAL
600mV
YA
YB
EXT
MAINS
AUTO
AC
DC
TRIG.
100kΩ
5pF
AMPL.
V/cm
mV/cm
BEAM SELECTOR
DC BAL.
POSITION
ILLUM.
FOCUS
INTENS.
POWER ON

The LF Oscilloscope in Practice

3

3.1. Measuring fast edges

When an ideal pulse, i.e. the rise time is zero, is applied to the oscilloscope input, one can still observe a certain transition time on the display. This means that the rise and fall times have increased from zero to a measurable value determined by the bandwidth of the Y amplifier of the oscilloscope used.

Suppose that the bandwidth is determined by an equivalent R and C at the input of the amplifier (see figure 3.1.).

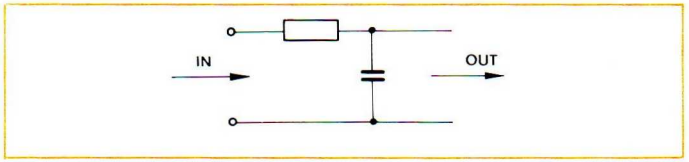


Fig. 3.1.

The bandwidth of this low-pass network will be

$$f_g = \frac{1}{2\pi RC} \text{ (to the —3 dB point).}$$

If we now apply an ideal pulse to the network, the output will be an exponential charging curve having the rise time $t_r = t_2\ (90\%) - t_1\ (10\%)$ as illustrated in figure 3.2.

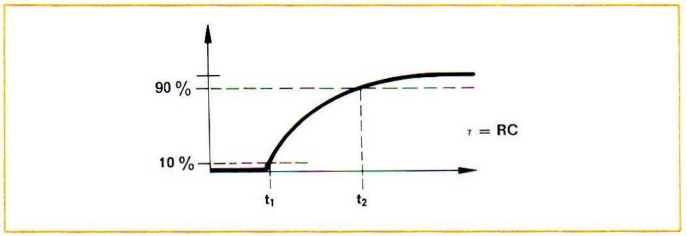


Fig. 3.2.

We can calculate t_r using the formula

$$t_r = RC\ln\frac{1}{0.1} - RC\ln\frac{1}{0.9} = RC\ln 9,$$

which gives $t_r = 2.2\ RC$.

By replacing RC with $\frac{1}{2\pi f_g}$ we obtain $t_r \times f_g = \frac{2.2}{2\pi} = 0.35$.

The rise time of an oscilloscope with the bandwidth 10 MHz (Philips PM 3232) will then be $0.35 \times 10^{-7} = 35$ ns.
An ideal step applied to this oscilloscope will thus be presented with the rise time 35 ns.

However, when measuring very fast edges one must also calculate with the rise time of cables, filters and attenuators used. The rise times of these devices are added according to the square-law rule.

Thus, the measured rise time t_{rm} will be

$$t^2_{rm} = t^2_{r\ generator} + t^2_{r\ cable} + t^2_{r\ oscilloscope}$$

The Philips pulse generator PM 5705 has a specified rise time of less than 10 ns and a 1 m piece of a highquality coaxial cable has a rise time of less than 1 ns; from these facts we can conclude that it is the oscilloscope that has the major influence on the reliability of the measurement.

Assuming $t_r \times f_g = 0.35$ and $t^2_{rm} = t^2_{r\ gen} + t^2_{r\ osc}$,

the influence of the oscilloscope on the measured rise time is illustrated in the following table:

Pulse rise time ns	Oscilloscope Bandwidth MHz	Oscilloscope rise time ns	Measured rise time ns	Error %
10	10	35	36.4	260
10	25	14	17.2	72
10	35	10	14.2	42
10	50	7	12.2	22
10	100	3.5	10.6	6
10	350	1	10.05	0.5
10	1000	0.35	10.01	0.1

Table 3.1.

3.2. Measurements at the upper frequency limit

The relations given in section 3.1. for the rise-time/bandwidth product and the square-law rule addition of rise times should be applied very restrictively when measuring a rise time much faster than that of the oscilloscope.

This will appear clearly from section 4.1., exercises 2 and 3, in which the rise and fall times are measured first with the output unloaded, then with a capacitive load to increase the rise and fall times. A low-frequency oscilloscope, the PM 3232, is compared with a high-frequency sampling oscilloscope, the PM 3400:

The calculated transition time $t_r = \sqrt{t^2_{rm} - t^2_{r\ osc}}$ or $t_f = \sqrt{t^2_{fm} - t^2_{r\ osc}}$

We can see that the fast sampling oscilloscope displays the real transition times. The calculated transition times are misleading because of the 35 ns rise time of the low-frequency oscilloscope. One exception is the fall time at 1000 pF load, which is 45 ns measured with the sampling oscilloscope and is calculated to 48.7 ns, i.e. an error of about 8 percent, which may be acceptable in some applications.

Consequently, when the rise and fall times of the pulse are increasing, the calculated rise time of the 10 MHz oscilloscope is approaching the real transition time measured with the sampling oscilloscope.

Load	PM 3232 (10 MHz, $tr_{r\ osc}$ 35 ns)				PM 3400 (1.7 GHz, $t_{r\ osc}$ 0.2 ns)	
	rise time ns		fall time ns		rise time ns	fall time ns
	measured	calculated	measured	calculated	measured	measured
	t_{rm}	t_r	t_{fm}	t_f	t_r	t_f
unloaded	40	19.4	40	19.4	8	13
470 pF	40	19.4	50	37.5	18	25
1000 pF	40	19.4	60	48.7	25	45

Table 3.2. Measuring the main pulse of PM 5705, 5 V into 50 ohm.


PHILIPS
REPETITION TIME
DURATION
DC OUTPUT
PM 3220

Applied Measurements

4.1. Pulse parameters

The definition of each parameter appears from figure 4.1. Particularly note the levels between which the measurements should be made. Note also that pulse droop and overshoot are stated as a percentage of the total amplitude.

The pulse spacing or the pulse repetition time is given in a suitable time unit. The inverted value of the pulse spacing is the pulse repetition frequency (PRF).

The duty factor is the relation between pulse duration and pulse spacing.

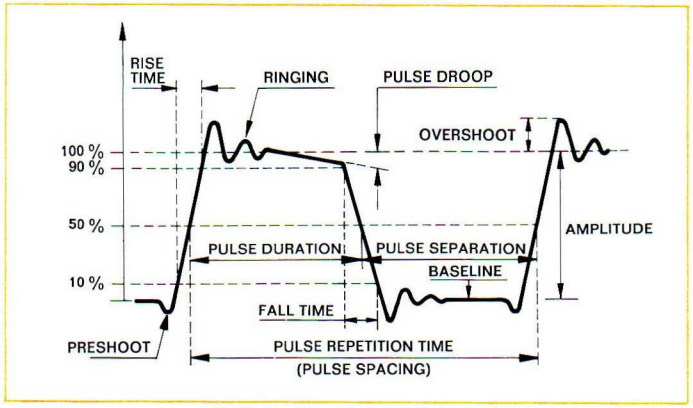


Fig. 4.1. Pulse parameters

Exercise 1

Preparatory measurement of pulse parameters

Equipment required:

1 pulse generator PM 5705 (PM 5704)
1 oscilloscope PM 3232
1 capacitor 15 nF
1 capacitor 47 pF
1 resistor 680 ohm

A majority of the pulse parameters can be visualized directly by measurements on the outputs of the pulse generator. If the outputs are loaded, certain pulse characteristics will be yet more emphasized and can be measured with a 10 MHz oscilloscope.

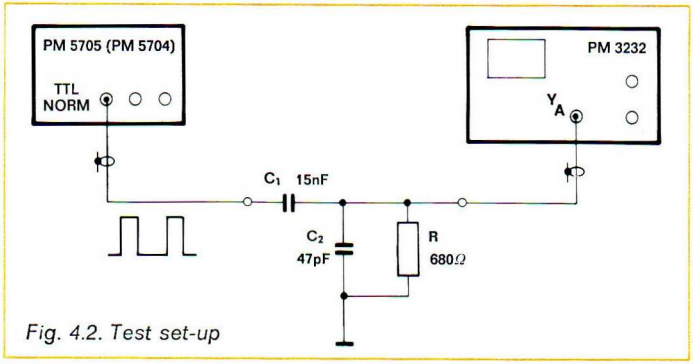


Fig. 4.2. Test set-up

Set the pulse generator:
DURATION 0.5 μs
REP.TIME 2.6 μs
Measure: pulse separation, duty factor, rise and fall time, overshoot and pulse droop.
Compare your result with the oscillogram fig. 4.3. Series capacitor C1 provides a pulse droop. Ringings are generated by parallel capacitor C2 together with stray inductances in the cables and the mismatch provided by the 680 ohm resistor.

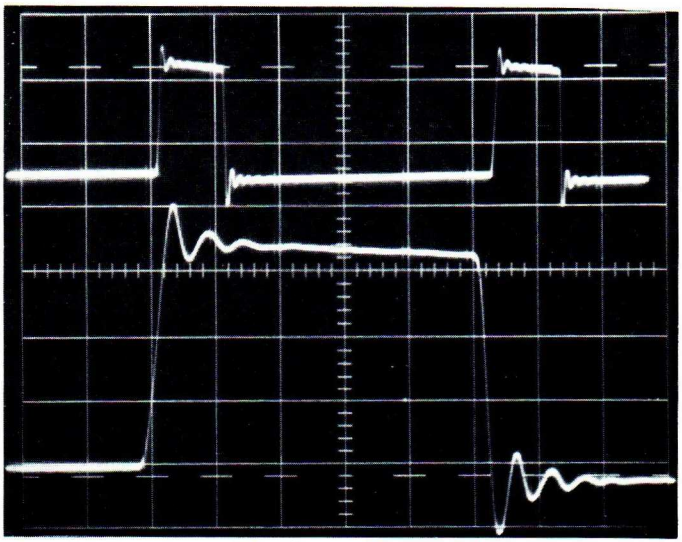


Fig. 4.3. Upper trace: 0.5 μs/cm. Duration 0.5 μs
Pulse separation 2.1 μs
Duty factor 0.19
Lower trace: 100 ns/cm. Rise and fall time 38 ns
Overshoot 14%
Pulse droop 4%

Exercise 2

Measuring the rise time of the main pulse of PM 5705

Equipment required:

1 pulse generator PM 5705
1 oscilloscope PM 3232
1 sampling oscilloscope PM 3400
1 termination 50 ohm, 1 W, PM 9585
1 BNC T-piece
1 capacitor 470 pF
1 capacitor 1000 pF
1 coaxial attenuator, 10 x (used in the sampling oscilloscope measurement)

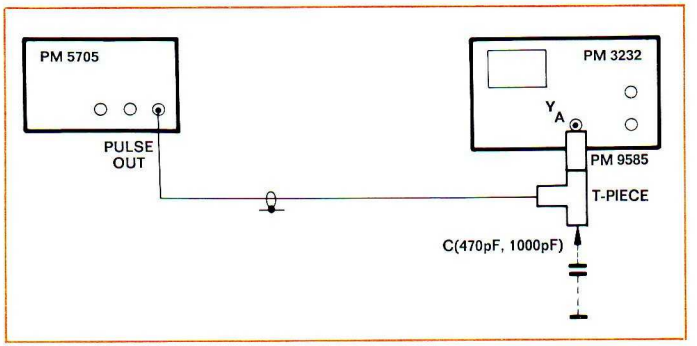


Fig. 4.4. Test set-up

Set the pulse generator:

AMPLITUDE	5 V
DURATION	1 μs
REP.TIME	2 μs
INT.LOAD	50 ohm

Set the oscilloscope:

TIME/cm	40 ns

Measure the rise time first with the generator output unloaded, then with 470 pF and 1000 pF capacitive load.

Calculate the rise time using the formula

$$t^2_r = t^2_{rm} - t^2_{r\ osc}$$

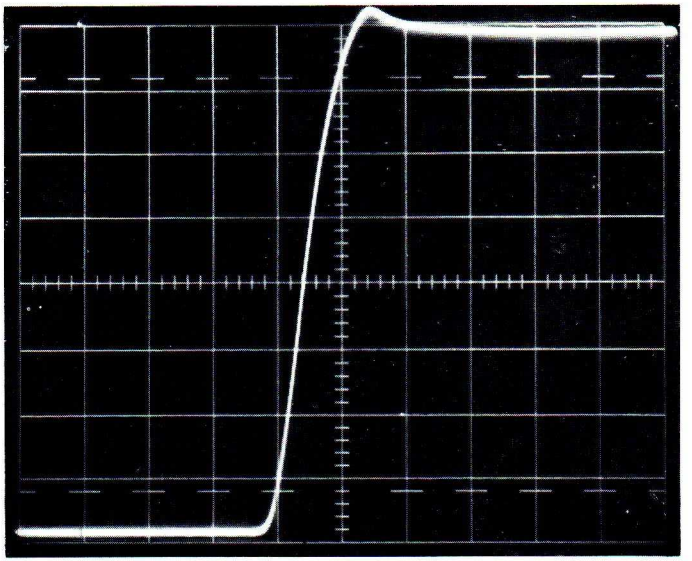


Fig. 4.5. PM 3232 Output unloaded: measured rise time t_{rm} = 36 ns

Load	Rise time ns	
	measured t_{rm}	calculated t_r
unloaded	40	19.4
470 pF	40	19.4
1000 pF	40	19.4

Change the test set-up (see fig. 4.6.)

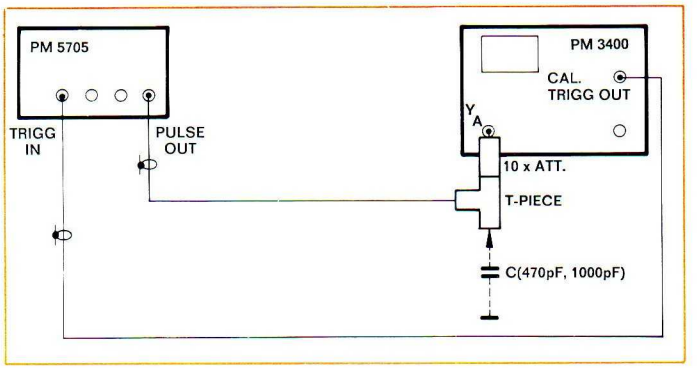


Fig. 4.6. Test set-up

Set oscilloscope controls: Set pulse generator:

TIME/cm	20 ns	REP TIME	EXT+
mV/cm	100 mV	AMPL	5 V
MAGNIFIER	5	DURATION	1 μs
		INT LOAD	50 ohm

Measure the rise time first with the generator output unloaded, then with 470 pF and 1000 pF capacitive load.

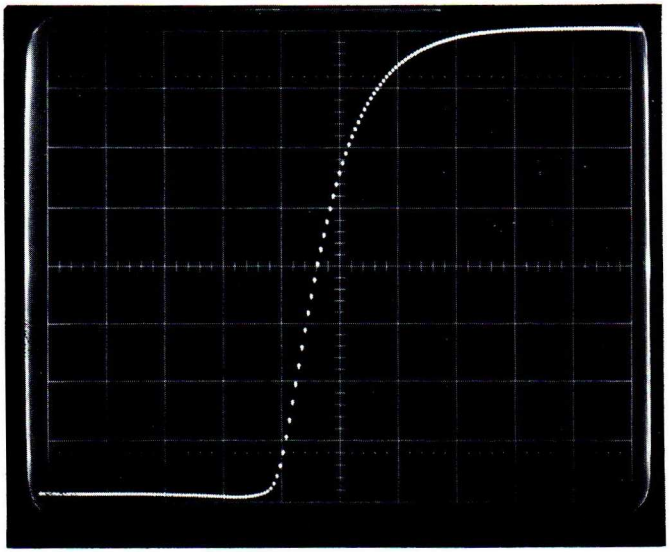


Fig. 4.7. PM 3400 Output unloaded: measured rise time t_{rm} = 8 ns

Load	Rise time ns measured
unloaded	8
470 pF	18
1000 pF	25

Table 4.2.

Exercise 3

Measuring the fall time of the main pulse of PM 5705.

Use the same equipment, set-up and procedure as in exercise 2, fig. 4.4. and 4.6. However, depress the COMPL. button of the PM 5705.

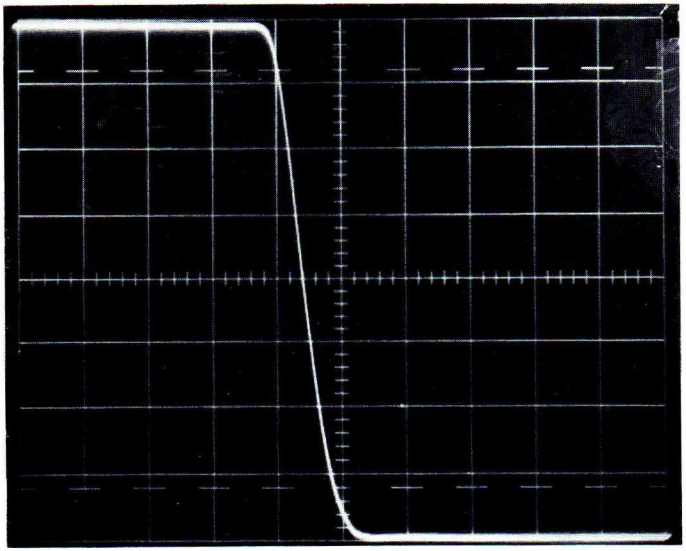


Fig. 4.8. PM 3232 Generator output unloaded Measured fall time 40 ns

Load	Fall time ns measured	calculated
unloaded	40	13.4
470 pF	50	37.5
1000 pF	60	48.7

Table 4.3.

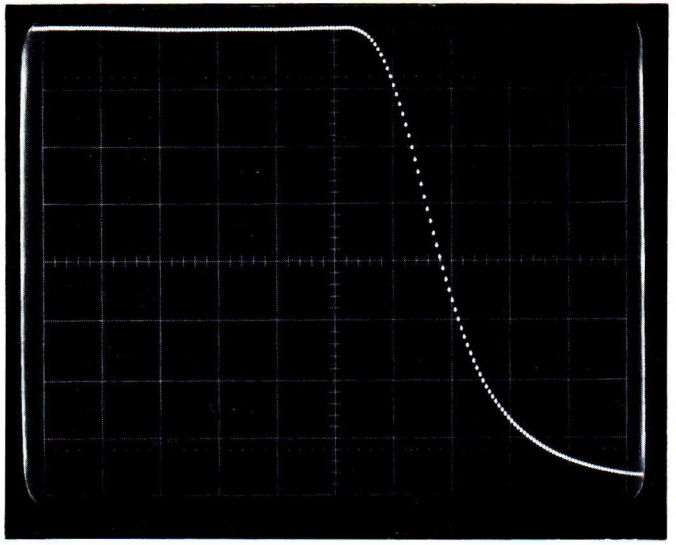


Fig. 4.9. PM 3400 Generator output unloaded
Measured fall time 13 ns

Load	Fall time measured
unloaded	13
470 pF	25
1000 pF	45

Table 4.4.

Exercise 4

Measuring the rise time of the TTL pulse of PM 5705 (or PM 5704)

Equipment required:

1 pulse generator PM 5705 (PM 5704)
1 oscilloscope PM 3232
1 sampling oscilloscope PM 3400
1 termination 50 ohm, 1 W, PM 9585
1 coaxial attenuator, 10 x
1 coaxial T-piece

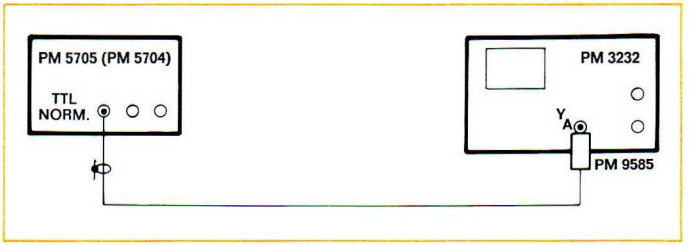


Fig. 4.10. Test set-up

Set the pulse generator:		Set the oscilloscope PM 3232:	
REP.TIME	2 μs	Ampl.A	0.2 V/cm
DURATION	500 ns	TIME/cm	40 ns

Measure the risetime and compare with the oscillogram fig. 4.11.

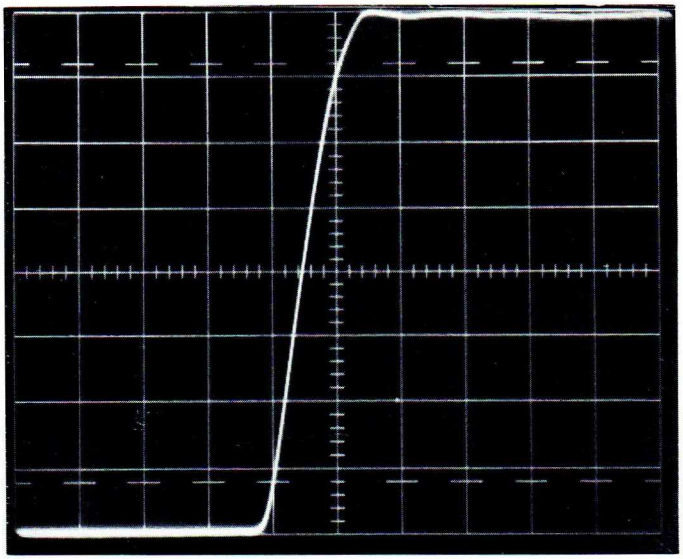


Fig. 4.11. PM 3232 Measured rise time 44 ns

Change the test set-up (see fig. 4.12.).

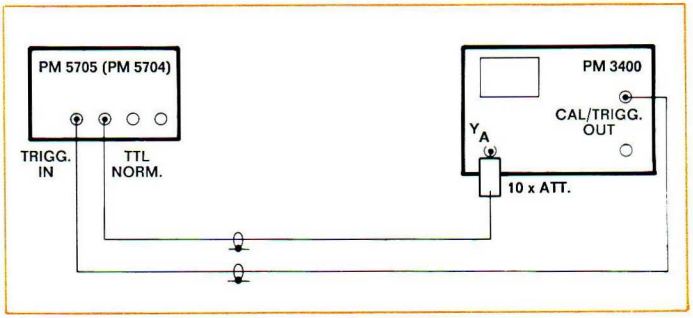


Fig. 4.12. Test set-up

Set the pulse generator:

REP.TIME	EXT —
DURATION	500 ns

Set the sampling oscilloscope:

TIME/cm	0.1 μs
MAGNIFIER	20
mV/cm	50

Measure the risetime and compare with the oscillogram fig. 4.13.

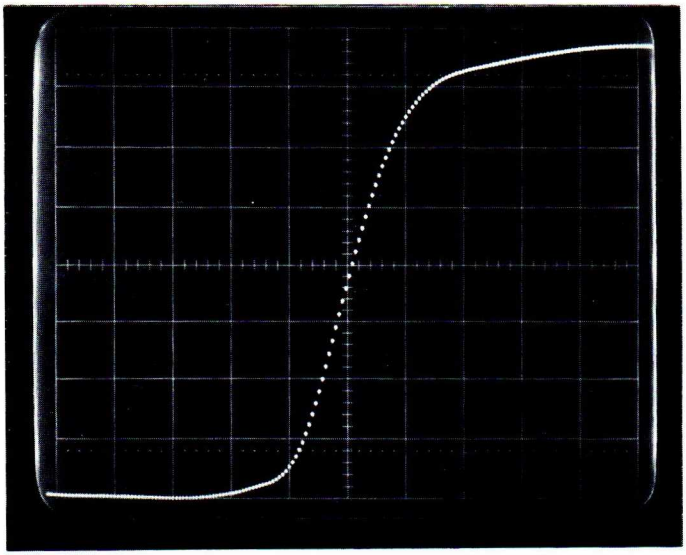


Fig. 4.13. PM 3400 Measured rise time 13 ns

Exercise 5

Measuring the fall time of the TTL pulse

Use the same equipment, test set-ups and procedure as in exercise 4.

Connect the measuring cable to the TTL COMPL. output. Measure with oscilloscopes PM 3232 and PM 3400 and compare your results with the oscillograms figure 4.14. and figure 4.15.

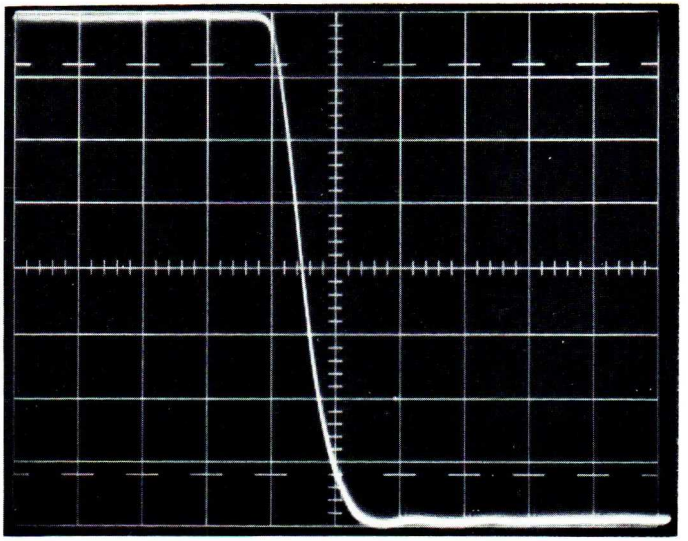


Fig. 4.14. PM 3232: measured fall time 36 ns

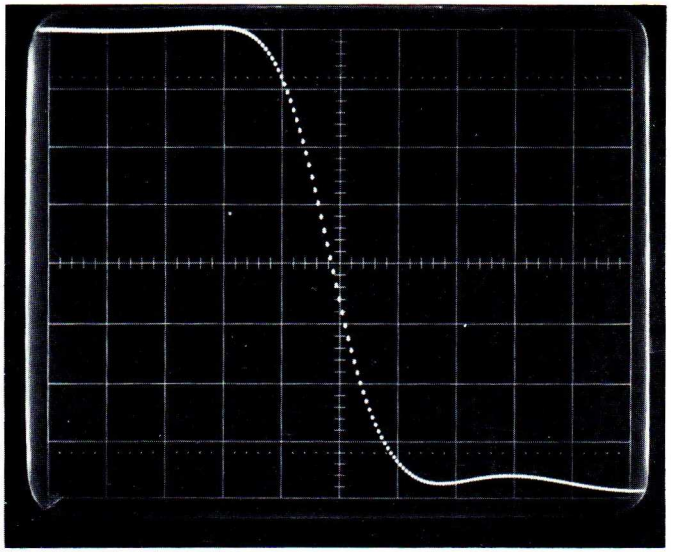


Fig. 4.15. PM 3400: measured fall time 9 ns

Exercise 6

Measuring the preshoot of a TTL pulse

Equipment required:

1 pulse generator PM 5705 (PM 5704)
1 oscilloscope PM 3232
1 DC power supply + 5 V (PM 5704 can be used)
1 IC SN 7400 with datasheet
1 capacitor 100 pF
1 resistor 680 ohm

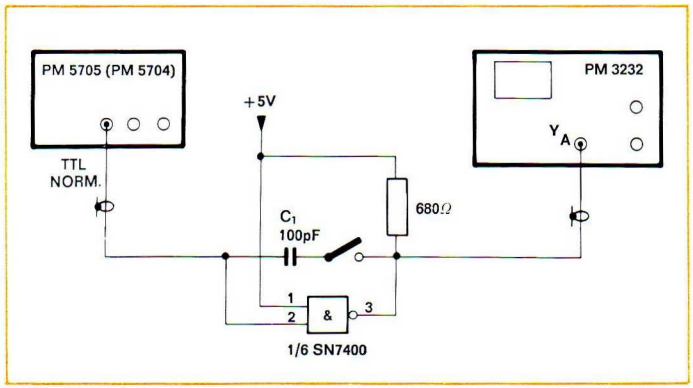


Fig. 4.16. Test set-up

Set the pulse generator:		Set the oscilloscope:	
REP.TIME	50 μs	TIME/cm	100 ns
DURATION	1 μs		

Preshoot is caused by capacitive coupling between the input and the output of an inverting stage.

Example: The output of a NAND gate is LOW and a negative step is applied to the input. This step will be partly transferred to the output via the stray capacitances before the output goes HIGH.

Measure the preshoot both with and without the shunting capacitor C_1. Compare your results with the oscillogram fig. 4.17.

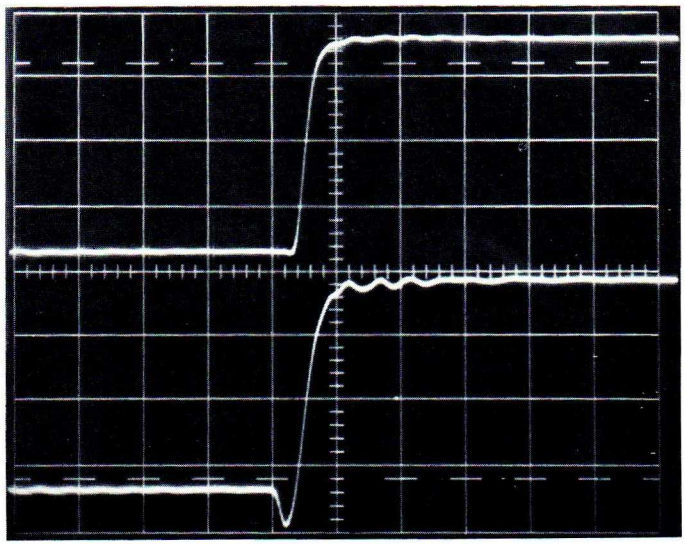


Fig. 4.17. Upper trace: without C_1 a small preshoot can be observed Lower trace: with C_1 connected the preshoot is 10% because the capacitance between input and output is increased.

4.2. Time Domain Reflectometry (TDR)

TDR can be used to study the properties of a transmission line e.g. a coaxial cable.

When a voltage step, V_i, is applied to a line, the source (the generator) sees in the first moment only the characteristic impedance Z_o of the line.

After a short period of time the leading edge of the step reaches the far end of the line, i.e. the load Z_L. If Z_L differs from Z_o there is a mismatch causing part of the incoming signal to reflect back to the source. The reflection V_r is determined by

$$V_r = \frac{Z_L - Z_o}{Z_L + Z_o} V_i$$

The velocity of a signal in a coaxial cable with small losses is in the order of 0.7 c, where c is the velocity of light, 3×10^8 m/s.

Assuming a cable length of L m, it will take $\frac{2\,L}{0.7\,c}$ seconds before the signal returns as a reflection to the source. The reflected signal "tells" the generator which type of impedance at the load end that can be expected when the transients have decayed. If the source impedance differs from the characteristic impedance, yet more reflections will occur before the generator adapts to its stationary value. Reflectometry can also be used to match the load impedance to an unknown cable or to trace a short-circuit or other discontinuity of a transmission line.

Exercise 7

TDR measurement

Equipment required:

1 pulse generator PM 5705
1 oscilloscope PM 3232
1 resistor 50 ohm } may be replaced by a 100 x
1 resistor 5 kohm } oscilloscope probe PM 9358
1 BNC T-piece
1 measuring cable, length > 10 m, 50 ohm, coaxial
2 resistors 50 ohm
1 capacitor 15 nF } Termination devices
1 inductance 0.1 mH
Connection cables, 50 ohm, coaxial.

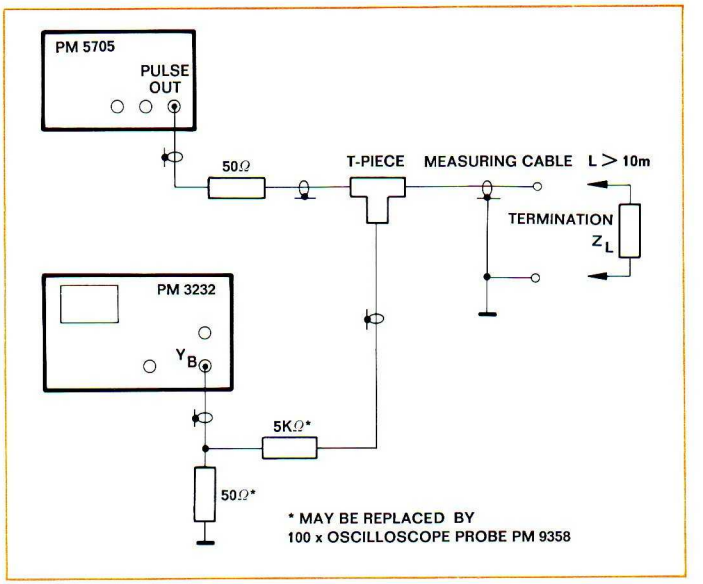


Fig. 4.18. Test set-up

Connect the pulse generator and the oscilloscope as illustrated in the set-up diagram fig. 4.18.

The output impedance of the pulse generator is 50 ohm (INT.LOAD depressed), but when the output transistor of the generator is on, the impedance is reduced. To ensure a permanent impedance of 50 ohm, which is particularly important at TDR measurements, an additional 50 ohm resistor is connected in series with the PULSE OUT output.

The connection of the oscilloscope must be high-ohmic (attenuation 100 x) to prevent interference in the measuring system. Furthermore, because the delay of the coaxial cable is about 5 ns/m, the length of the measuring cable should exceed 10 m. In the oscillograms figures 4.21., 4.24., 4.27., the measuring cable was 50 m.

Set the pulse generator:		Set the oscilloscope:	
AMPLITUDE	5 V	TIME/cm	0.2 μs
DURATION	5 μs	AMPL.	20 mV/cm
REP.TIME	10 μs		
INT.LOAD	50 ohm		

a. Measure the reflections when the line is open.

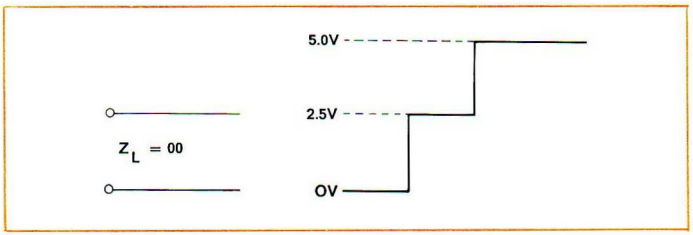


Fig. 4.19. Open line

Then compare with the result obtained when the far end of the line is shorted.

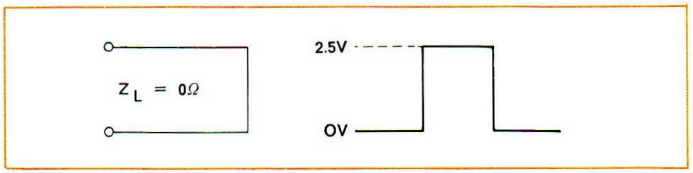


Fig. 4.20 Far end shorted

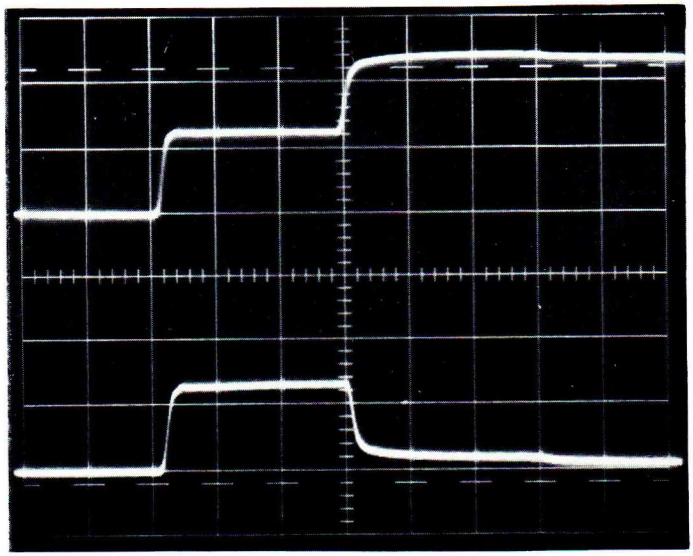


Fig. 4.21. Upper trace: open line
Lower trace: far end shorted

b. Measure the reflections when the line is terminated with a 50 ohm resistor.

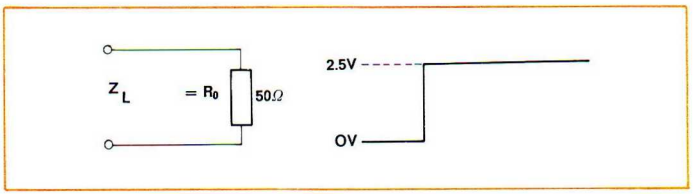


Fig. 4.22. 50 ohm termination

Next, terminate with two 50 ohm resistors connected in series.

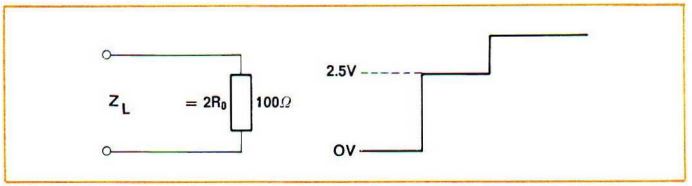


Fig. 4.23. 100 ohm termination

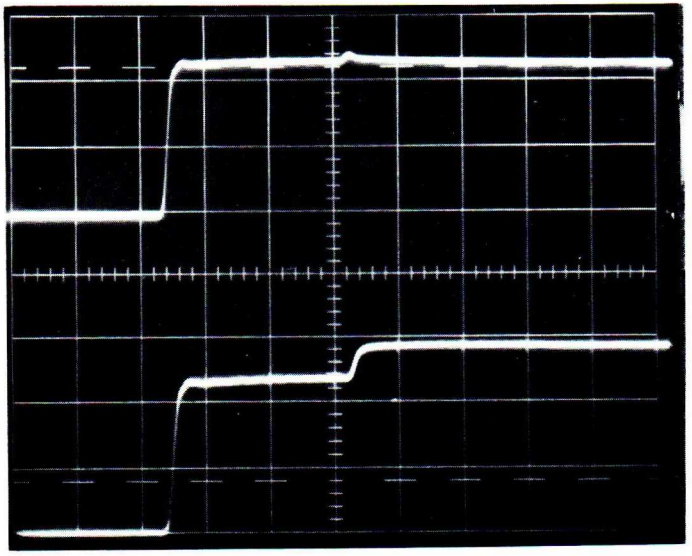


Fig. 4.24. Upper trace: 50 ohm termination
Lower trace: 100 ohm termination

c. Measure the reflections caused by an RC termination, 50 ohm in parallel with 15 nF.

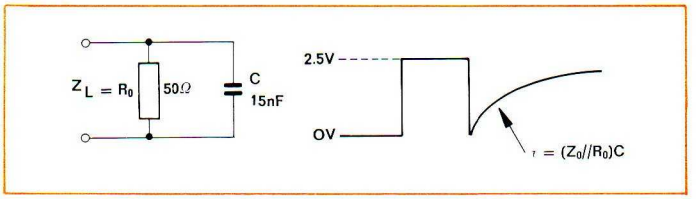


Fig. 4.25. RC termination

Terminate with an RL network, 50 ohm in series with 0.1 mH.

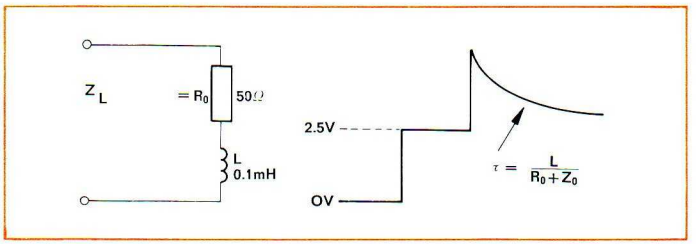


Fig. 4.26. RL termination

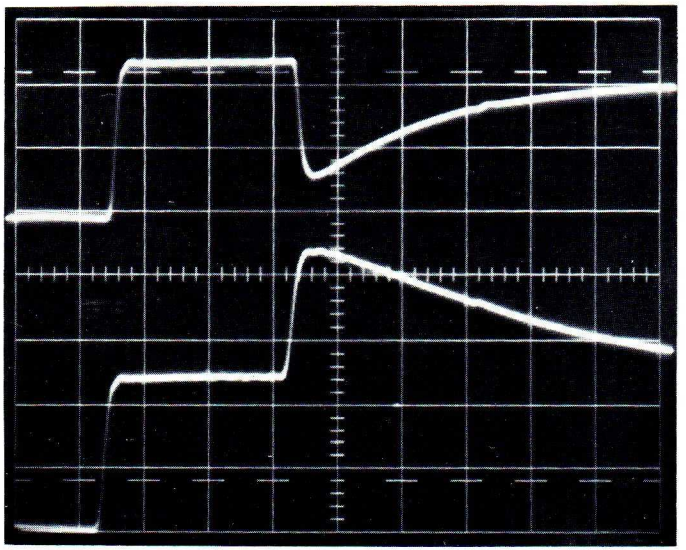


Fig. 4.27. Upper trace: RC termination
Lower trace: RL termination

4.3. Line equivalents

When measuring fast pulse events it is important to know the fault sources that can affect the measuring result. The device under test should not be judged on the basis of an oscilloscope representation until it has been carefully analysed how the test set-up is influencing the waveforms.
Long and unsuitable test cables are one of the most common reasons for false measuring results.

Each cable has a certain resistance, inductance and capacitance per meter, which can easily be verified using an impedance bridge. Note that the significant inductance originates from a current loop, i.e. both from the forward and the back (earth) conductor in the set-up. See fig. 4.28.

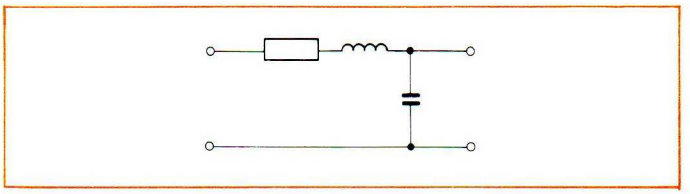


Fig. 4.28.

The simplest equivalent for a line consists of R, L and C. The component values are varying considerably depending on conductor area, the dielectric properties of the insulation, the physical construction, the location in the measuring room etc.

The following values have been measured for a common, plastic insulated laboratory cable, 1.5 m of length, area 2 mm², and a coaxial cable type RG58C/U of equal length:

	Parallel conductors approx. 1 cm distance	Twisted approx. 2 turns/10 cm	RG58C/U
R*	0.13 ohm	0.13 ohm	0.11 ohm
L*	2.3 μH	1.3 μH	0.6 μH
C	20 pF	100 pF	199 pF

* Remote end shorted

Exercise 8

Measuring the influence of the cables on the waveform

Equipment required:

1 pulse generator PM 5705
1 oscilloscope PM 3232
1 termination 50 ohm, PM 9585
2 BNC to banana plug adapters
2 wires, length 1.5 m (exercise 8a)
2 twisted wires, length 1.5 m (exercise 8b)
1 coaxial cable, BNC terminated, 50 ohm (exercise 8c)
2 wires, length about 20 cm (exercise 8d)
1 resistor 0.1 ohm } (to be constructed, see below) } (exercise 8e)
1 inductance 1.2 μH }
1 capacitor 100 pF

Set the pulse generator:		Set the oscilloscope:	
AMPLITUDE	2 V	AMPL. A	2 V/cm
REP.TIME	3 μs	TIME/cm	0.2 μs
DURATION	0.75 μs		
INT.LOAD	50 ohm		

Make the following measurements test set-ups 4.29., 4.31., 4.33., 4.35. and 4.37. Note the influence of 50 ohm termination. Compare with the oscillograms.

a) Parallel measuring cables

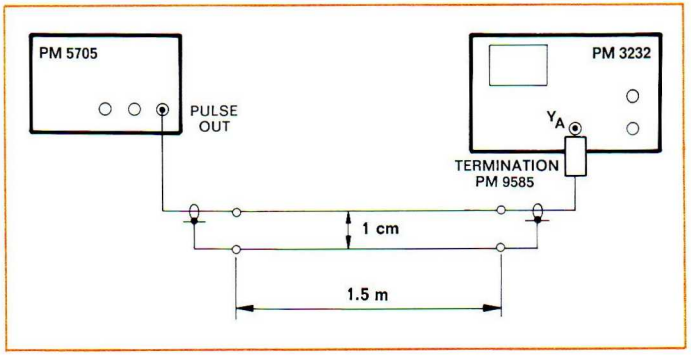


Fig. 4.29. Test set-up

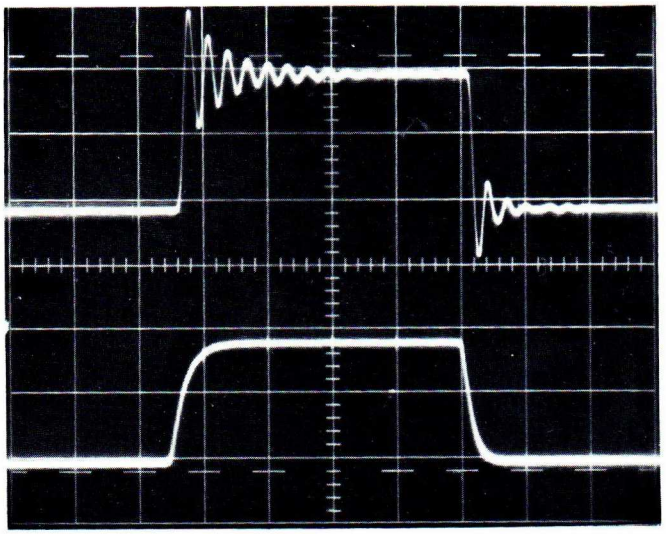


Fig. 4.30. Upper trace: Unterminated cables
Lower trace: Cable is terminated with 50 ohm at oscilloscope end. Note that ringings are damped.

b) Twisted measuring cables

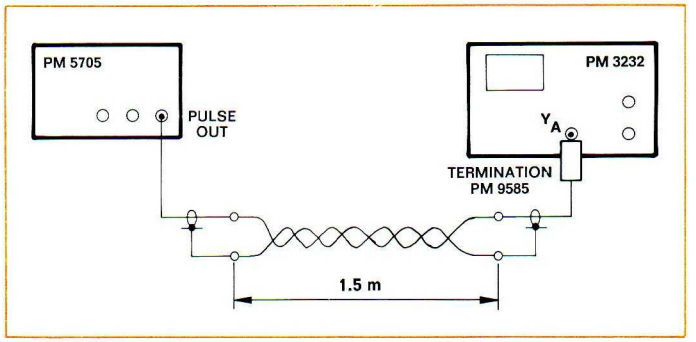


Fig. 4.31. Test set-up

c) Coaxial cable RG58C/U

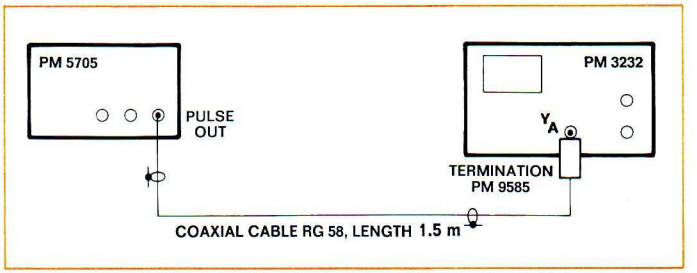


Fig. 4.33. Test set-up

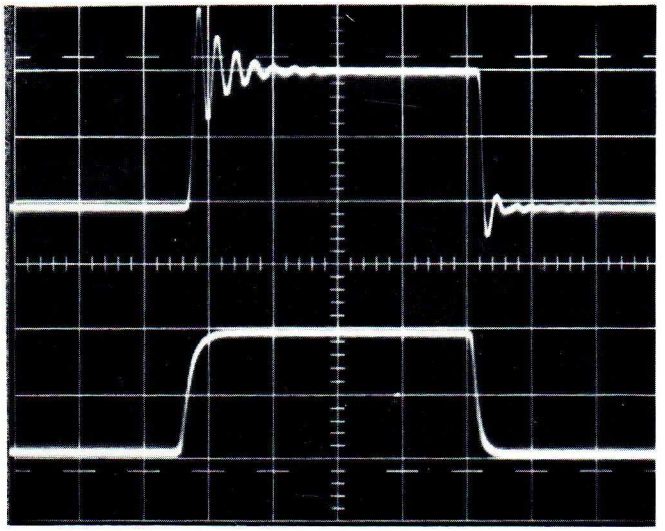


Fig. 4.32. Upper trace: Unterminated cables
Lower trace: 50 ohm terminated cables. Ringings are damped.

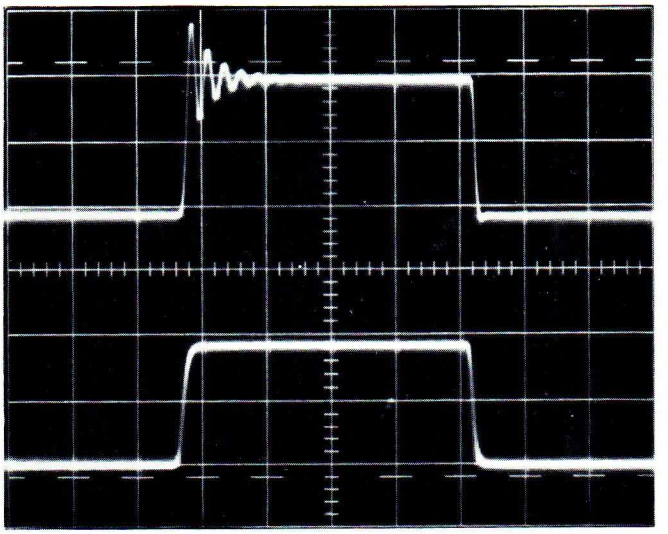


Fig. 4.34. Upper trace: Still overshoots without termination. Matching improved at negative step.
Lower trace: Terminated with 50 ohm.

d) Short measuring cables

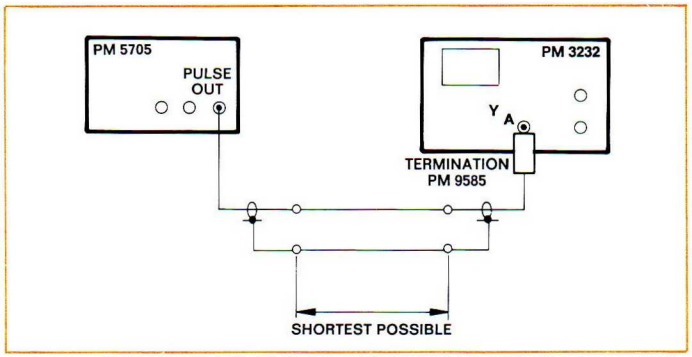


Fig. 4.35. Test set-up

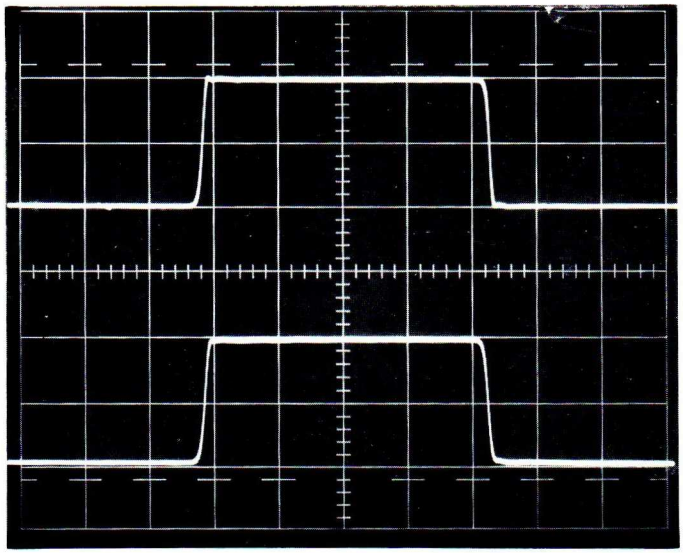


Fig. 4.36. Upper trace: Unterminated cables.
Lower trace: Cables terminated with 50 ohm at oscilloscope.

Conclusion: As short measuring cables as possible gives the best result.

e) Artificial line

The inductance and the resistance is about 25 turns of a 0.4 mm wire around a common pencil. Use as short connection cables as possible.

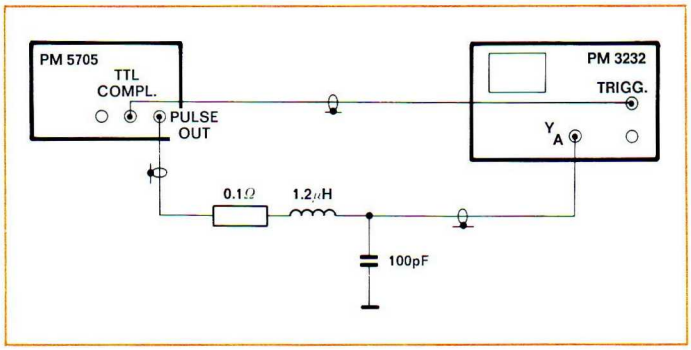


Fig. 4.37. Test set-up

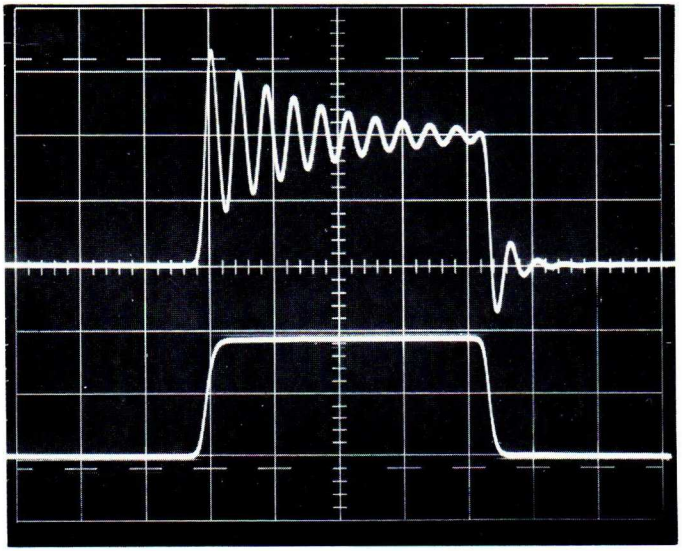


Fig. 4.38. Upper trace: Unterminated
Lower trace: Terminated with 50 ohm

Note that ringings are damped by the 50 ohm termination!

4.4. Recovery time of a power diode

In a dc voltage source for high power the chopper technique is often used to increase the frequency at the primary side of the transformer. With this approach, the size of the iron core of the transformer is reduced, because the size is proportional to 1/f.

Thus the voltamperes per weight unit of transformer can be increased. See fig. 4.39.

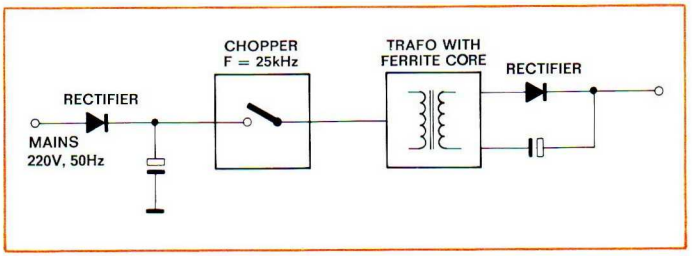


Fig. 4.39.

When the frequency is increased the recovery time of the diode may be troublesome. The diode does not turn off immediately, but reverse current is flowing during a certain period of time causing ripple on the voltage across the capacitor.

The recovery time of the diode when the voltage is reversed depends on the charge distribution in the PN junction. The diode current in the forward direction will also provide a certain amount of stored excess charge in the PN junction.

When the voltage across the diode is reversed, this charge must be removed before the diode can cease conducting.

Then the reverse current is decreasing exponentially when the PN junction is reversed and the minority carriers are depleted.

Exercise 9

Determining the recovery time of a power diode

Equipment required:

1 pulse generator PM 5705
1 oscilloscope PM 3232
1 capacitor 2.2 μF
2 resistors 50 ohm
1 power diode IR 10D4

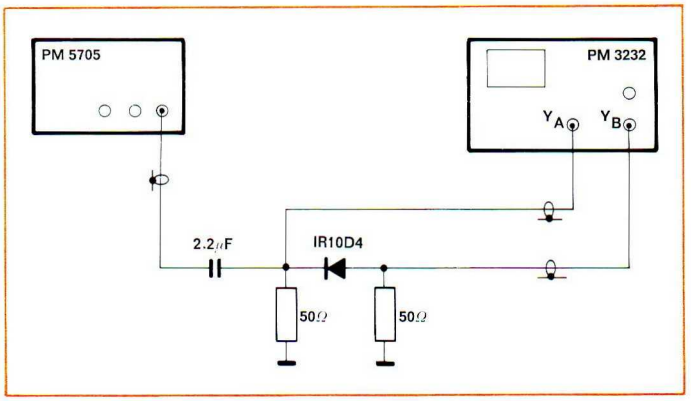


Fig. 4.40. Test set-up

Set the pulse generator:		Set the oscilloscope:	
AMPLITUDE	7.5 V	AMPL. A	2 V/cm
DURATION	5 μs	TIME/cm	2 μs
REP.TIME	10 μs		
INT.LOAD	50 ohm		

To obtain a square wave symmetrical around the zero level, a capacitor should be series connected with the pulse generator. The current through the diode is measured across a 50 ohm resistor. Measure the recovery time.

Compare your result with the oscillogram fig. 4.41.

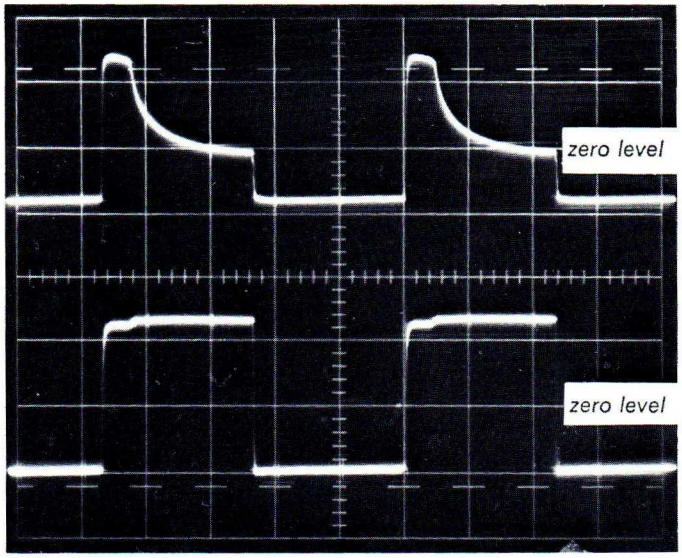


Fig. 4.41. Upper trace, ch. B: diode current. Forward current approx. 35 mA.
Lower trace, ch. A: voltage across load.

The recovery time is about 5 μs.
The current-time area above the zero level corresponds to the charge that must be removed before the diode can cease conducting.

4.5. Transients on the TTL supply voltage

When a TTL circuit is switching from LOW to HIGH, transients are occuring on the supply voltage because the TTL totem pole output, when going HIGH, is short-circuiting the supply voltage during a short moment. See fig. 4.42.

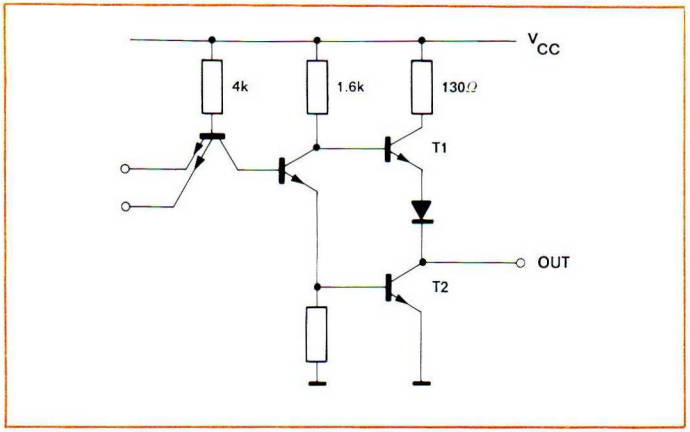


Fig. 4.42. Circuit diagram of a TTL output

When the TTL output goes from the LOW to the HIGH state, transistor T_2 is turned off and T_1 goes on.

Since the recovery time of a saturated transistor is longer than its switch-on delay, both T_1 and T_2 will conduct simultaneously during a short moment. The current will then be limited only by the 130 ohm resistor.

The current spike can be maximum

$$\frac{V_{CC} - 2 \times V_{SAT} - V_{DIODE}}{130}$$

in which V_{SAT} is the voltage across the saturated transistor.

Thus, the current spike is: $\frac{5 - 2 \times 0.5 - 0.7}{130} \approx 25$ mA

If several gates switch simultaneously, the current spike on the supply line is increased linearly with the number of gates. These spikes can easily trigger fast TTL circuits and be quite fatal, e.g. destroy the information stored in a memory (refer to exercise 11).

Exercise 10

Transients on the TTL supply voltage

Equipment required:

1 pulse generator PM 5705 (PM 5704)
1 oscilloscope PM 3232
1 d.c. power supply
1 IC SN 7400 with datasheet
1 capacitor 0.1 μF
1 resistor 600 ohm
1 capacitor 15 pF
1 BNC T-piece
1 50 ohm termination PM 9585

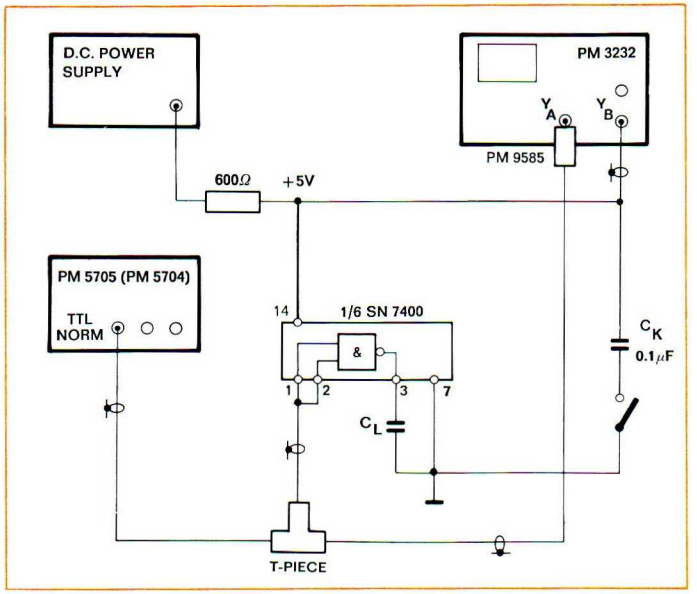


Fig. 4.43 Test set-up

Set the pulse generator:

DURATION	0.5 μs
REP.TIME	1 μs

Set the oscilloscope:

TIME/cm	0.2 μs
AC coupled	
AMPL. A	2 V/cm
AMPL. B	1 V/cm

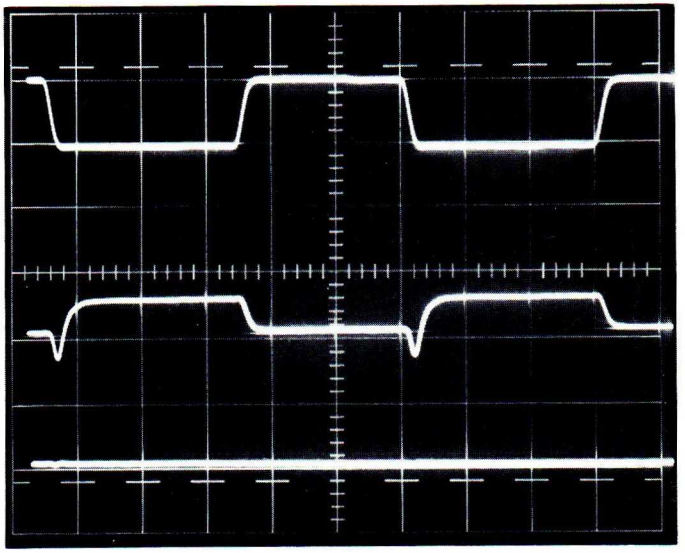


Fig. 4.44. Upper trace: Channel A, input signal
Middle trace: Channel B, supply voltage, without C_k
Lower trace: Channel B, supply voltage, with C_k

The 600 ohm resistor is series connected with the power source to make the supply high-ohmic. This will emphasize the different currents at HIGH and LOW input. Note that the current spike is obtained only when the input goes LOW. The capacitive load C_L will increase the amplitude of the current spike. The decoupling capacitor C_K should be chosen to 0.1 μF for each group of 5 TTL packages.

Possibly, two capacitors of different types can be parallel connected: one ceramic type which can provide much current, and one electrolytic type having relatively great loss and being capable of damping the ringings which otherwise can occur in the LC circuit formed by the supply line.

Exercise 11

Faults in a memory caused by interfering transients

An RS flip-flop (see section 4.6. exercise 14 and fig. 4.45.) can be regarded as a memory. Its stored information, 1 or 0, can be destroyed by an interfering pulse applied via the supply voltage.

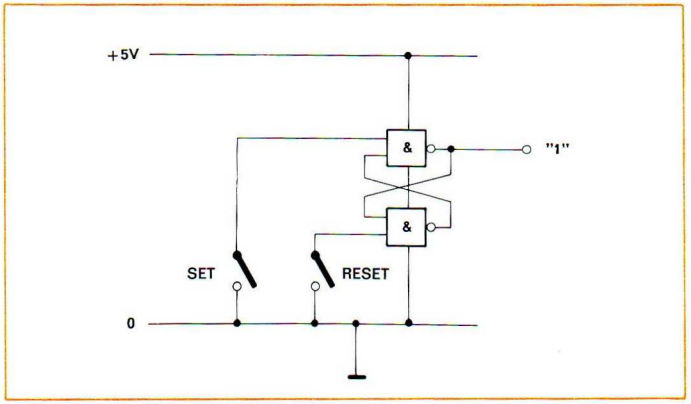


Fig. 4.45. RS flip-flop

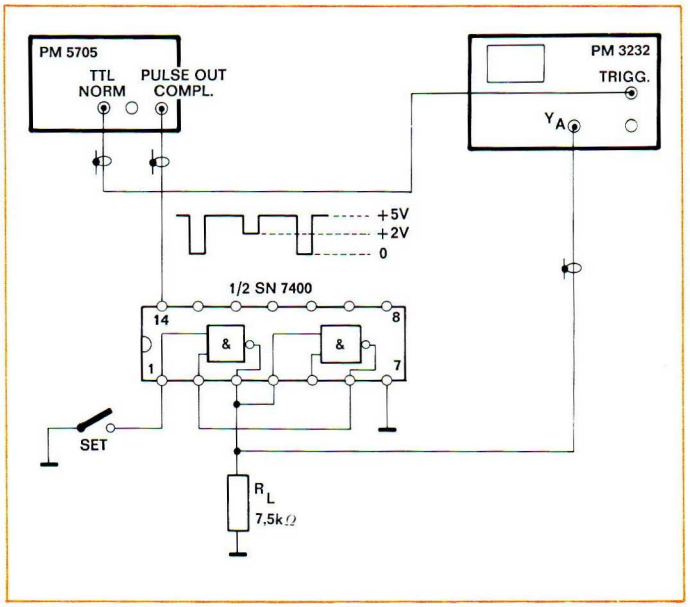


Fig. 4.46. Test set-up

If a flip-flop is connected to the supply voltage it will be set to either of its both states 1 or 0.

Theoretically this will occur quite randomly, but in practice the two inputs are not identical because of stray capacitances. Therefore, the flip-flop will always be set to the same state each time it is connected to the supply voltage.

Equipment required:

1 pulse generator PM 5705
1 oscilloscope PM 3232
1 IC SN 7400 with datasheet
1 resistor 7.5 kohm

Set the pulse generator:

AMPL.	5 V
DURATION	2 μs
REP.TIME	1 to 5 s
NORMAL/COMPL.	COMPL.
DC OFFSET	+2 V

Set the oscilloscope:

TIME/cm	1 μs
AMPL.	1 V/cm
EXT. TRIGG	+
DC-coupled	

Set the RS flip-flop to the state opposite to its normal one at the connection to the supply voltage.
R_L corresponds to the maximum load for TTL circuits with fan-out = 10.

The supply voltage with superimposed transients is now represented by the complementary pulse train from the generator. By varying the baseline offset the amplitude of the negative-going interference pulses can be set between 5 V and 3 V. Vary also the duration and note the influence.

After each interference pulse the flip-flop must be manually set to "1".

4.6. Contact bounces

When a relay is used to switch TTL circuits the contact bounces must be taken into consideration.
The TTL circuits are fast enough to count the bounces just as if they were a pulse train.

If one wants to count the number of switchings of a relay, the result would be completely false unless the contact bounces are eliminated.

Exercise 12

Contact bounces

A common micro-relay can be used up to about 300—400 Hz and requires about 100 mW to switch. The PM 5705 pulse generator supplies max. 15 V, 300 mA at the main pulse output and can very well be used as the driving source.

Equipment required:

1 pulse generator PM 5705
1 oscilloscope PM 3232
1 micro-relay without diode across the winding
1 BNC T-piece

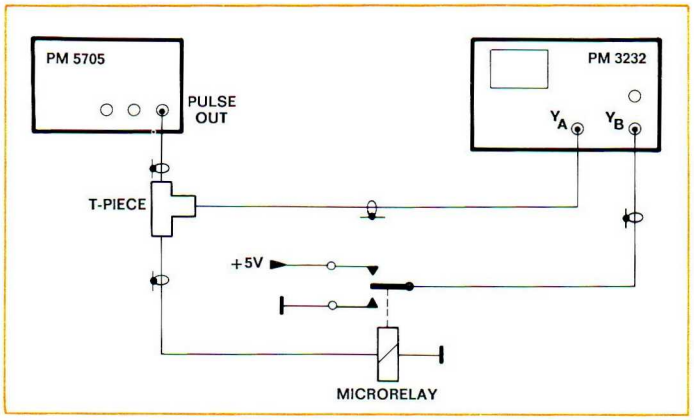


Fig. 4.47. Test set-up

Set the pulse generator:

AMPL.	5 V
DURATION	20 ms
REP.TIME	30 ms

Set the oscilloscope:

TRIGG YA	"+"
TIME/cm	200 μs
AMPL. A	1 V/cm

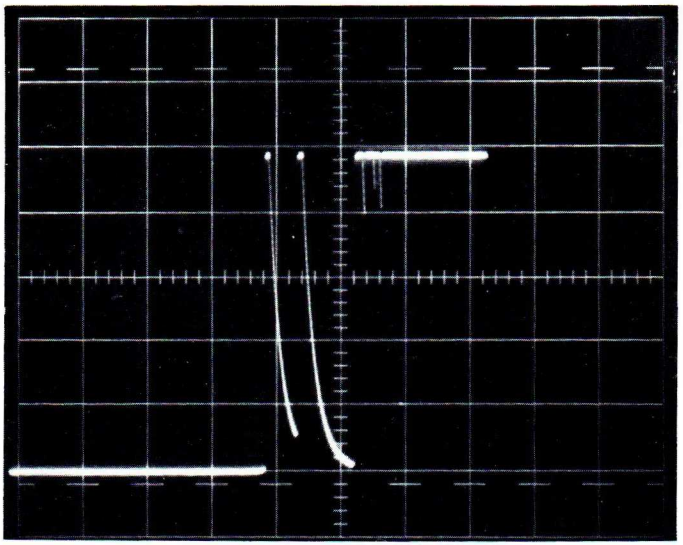


Fig. 4.48. The micro-relay turns on. Spacing between contact bounces is about 0.1 ms i.e. a frequency of 10 kHz.

Exercise 13

This exercise will verify that contact bounces are easily triggering a TTL circuit.

Use the same equipment as in exercise 12, but add one resistor 680 ohm, one IC SN 7400 and a d.c. power supply +5 V (PM 5704 can be used).

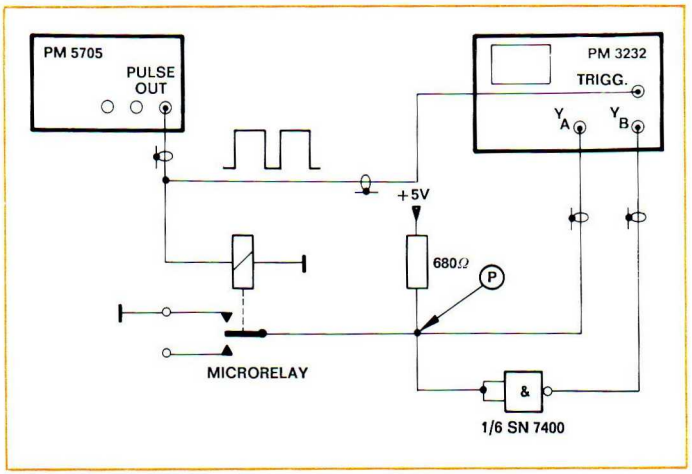


Fig. 4.49. Test set-up

Set the pulse generator:		Set the oscilloscope:	
AMPL.	5 V	TRIGG.	EXT+
DURATION	20 ms	COUPL.	AC
REP.TIME	30 ms	TIME/cm	200 μs
		AMPL.	2 V/cm

Compare the contact bounces with the output of the TTL-gate (see fig. 4.50.).

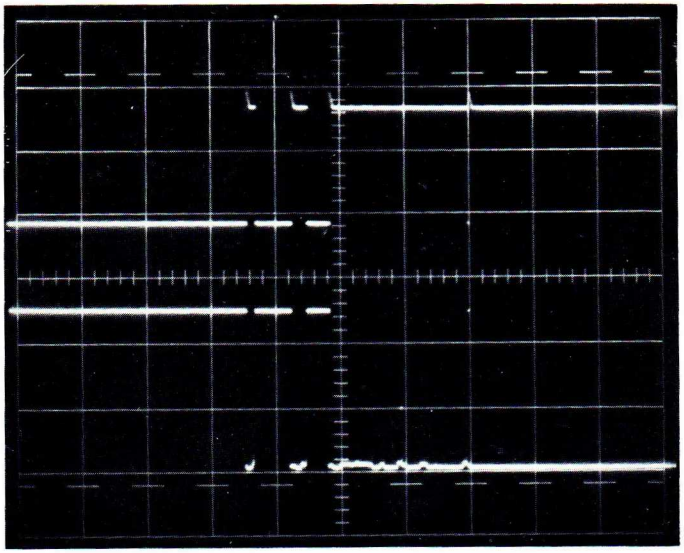


Fig. 4.50. Upper trace, channel B: The gate registers three pulses Lower trace, channel A: Contact bounces. The voltage at point P in the set-up diagram fig. 4.49. is switching between 5 and 0V

Exercise 14

With the aid of an RS flip-flop, consisting of two NAND gates, the contact bounces can be eliminated and the result is a clean pulse.

Equipment required:

1 pulse generator PM 5705
1 oscilloscope PM 3232
1 micro-relay without diode across the winding
2 resistors 680 ohm
1 resistor 10 ohm
1 IC SN 7400 with datasheet
1 power supply +5 V (PM 5704 can be used)
1 BNC T-piece

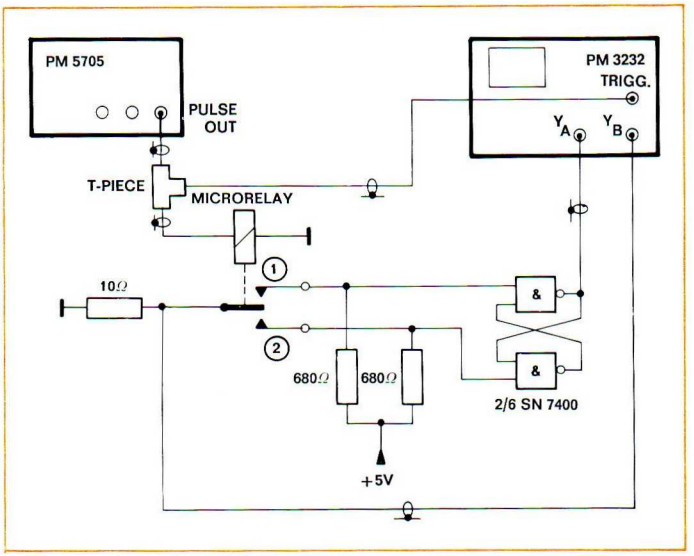


Fig. 4.51. Test set-up

Set the pulse generator:		Set the oscilloscope:	
AMPL.	5 V	TIME/cm	5 ms
DURATION	20 ms	AMPL. A	2 V/cm
REP.TIME	30 ms	AMPL. B	20 mV/cm
		EXT. TRIGG	+
		AC coupled	

Compare the contact bounces with the output of the RS flip-flop.

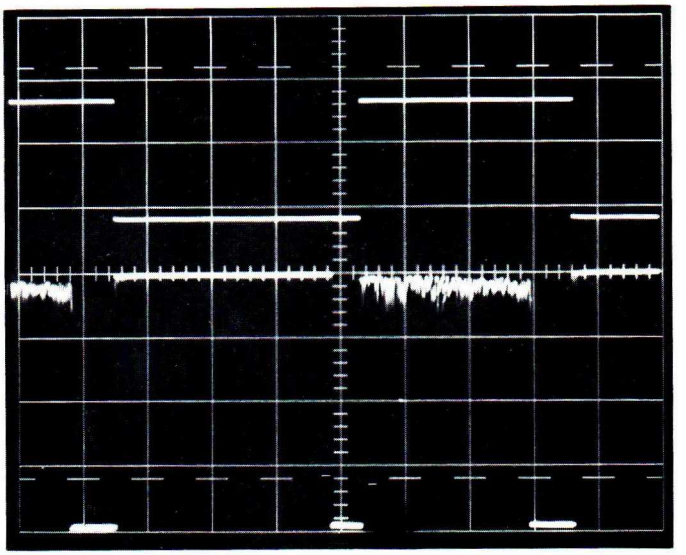


Fig. 4.52. Upper trace: (channel A) the output signal of the RS flip-flop
Lower trace: (channel B) the voltage across the 10 ohm resistor. The negative pulses correspond to the movement of the relay reed between positions 1 and 2 in the circuit diagram fig. 4.51. (approx. 3 ms)

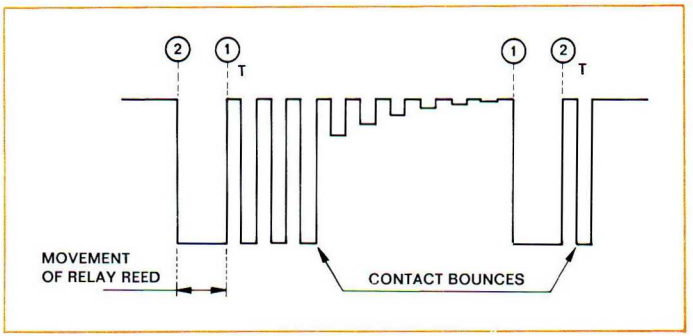


Fig. 4.53. Notice how the RS flip-flop is triggering on the very first contact at position 1_T and 2_T respectively.

4.7. The "current sink" concept

A TTL gate being connected to a pulse generator will consume a certain amount of current, whose direction and magnitude depend on the logic state of the gate. The specified current consumption for each input of one of the inverters in SN 7404 is 40 μA when the logical level at the input is HIGH (I_{IH} = input HIGH). If the input is connected to a logical "0" the gate provides maximum 1.6 mA, that is, (I_{IL} = input LOW) — 1.6 mA.

Consequently, the pulse generator used must accept this current to be able to decrease the input of the gate to the LOW level. This means that the output impedance of the generator or the gate must be low enough to permit the product $R_{out} \times I_{IL}$ being lower or equal to the transition level of a subsequent gate.

This is referred to as the current sink concept.

The average transition level is 1.4 V but may vary between 0.8 V and 2.0 V.
I_{IL} = — 1.6 mA, being specified in the data sheets, is the absolute maximum value. An average value is about — 1 mA.

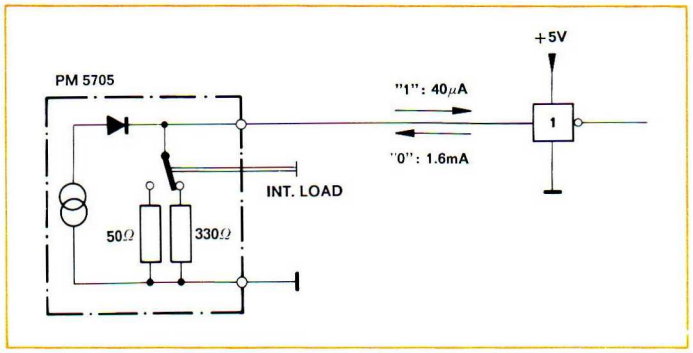


Fig. 4.54.

We can verify how a TTL gate is dependent of a low generator impedance by means of the PM 5705. The main output (pulse out) is arranged as indicated in figure 4.54. The generator impedance can be selected to 330 ohm or 50 ohm by means of button INTERNAL LOAD.

Exercise 15

Preparatory measurement of fanout.

Equipment required:

1 pulse generator PM 5705
1 oscilloscope PM 3232
2 IC's SN 7404 with datasheet
1 d.c. power supply +5 V (PM 5704 can be used)
1 BNC T-piece

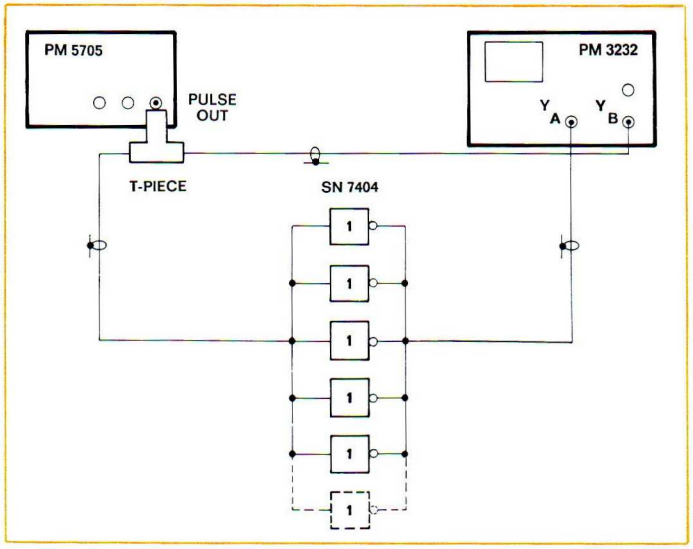


Fig. 4.55. Test set-up

Set the pulse generator:		Set the oscilloscope:	
AMPL.	3 V	AMPL.	1 V/cm
REP.TIME	15 μs	TIME/cm	5 μs
DURATION	5 μs	TRIGG	B
INT.LOAD	330 ohm		

Connect the pulse generator as shown in the set-up diagram fig. 4.55. and load the output with a number of parallel inverters of the SN 7404 type. Notice on the B channel of the oscilloscope how the logical "0" level of the generator voltage is increasing proportionally to the number of connected inverters.

When 9 to 10 parallel inverters are used, the "0" level exceeds about 1.4 V and the inverters cease triggering. This

can be observed on channel A of the oscilloscope.
Measure the low level threshold with the baseline offset.

Assuming that the logical "0" level is 1.5 V, and 10 inverters are used, I_{IL} for each inverter can be calculated:

$$10 \times I_{IL} = \frac{1.5\ V}{330\ \Omega} \qquad I_{IL} = 0.45\ mA$$

Next, depress button INTERNAL LOAD to 50 ohm. Note that the inverters are triggering again, because of the low impedance (current sink!).

Exercise 16

Verify importance of low source impedance for TTL-drivers due to current sink.

Use the same equipment and set-up as in exercise 15, but replace the two IC's SN 7404 by one decade counter SN 7490.

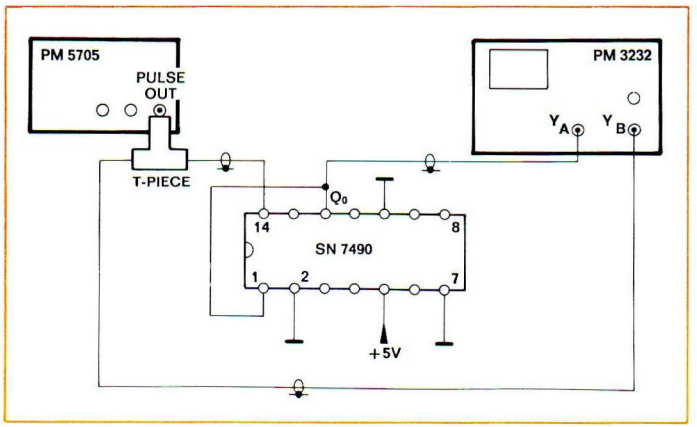


Fig. 4.56. Test set-up

Set the pulse generator:

AMPL.	3 V
DURATION	5 μs
REP.TIME	15 μs
INT.LOAD	330 ohm

Set the oscilloscope:

TIME/cm	5 μs
AMPL. A	1 V/cm
AMPL. B	1 V/cm

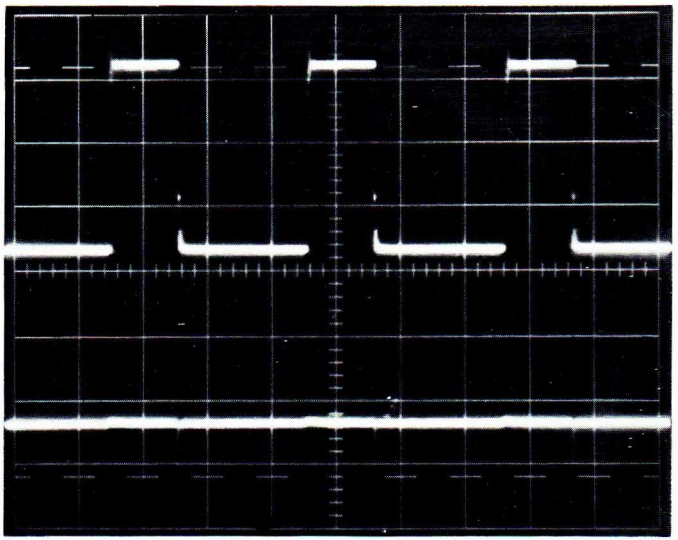


Fig. 4.57.

Upper trace; Ch. B: input signal 1V/cm 5 μs/cm
Generator impedance for logical "0" is 330 ohm.
Lower trace; Ch. A: Q_0 is permanently logical "1". Fast transients at the moment of transition are disregarded.

Depress INT.LOAD to 50 ohm and notice that Q_0 is triggering properly. Measure the low level threshold with the baseline offset.

I_{IL} = 3.2 mA specified in the datasheet of the SN 7490, is an absolute maximum value. As the increase of the "0" level can be measured on the oscilloscope, we can calculate I_{IL} to 0.4 V/330 ohm = 1 mA.

With the aid of the calculated I_{IL} values it is possible to state fan-out, see table 4.5. Complete the table 4.5.

LOW state generator fan-out					
IC type (load)		pulse out 330 Ω	Pulse out 50 Ω	Pulse out 50 Ω + ext. 50 Ω	TTL out
SN 7404	Measured	5—7			
	Specified	1	10	20	30
SN 7490	Measured	0—1			
	Specified	0	5	10	15

Table 4.5.

Measure the low level threshold with the baseline offset.

One can immediately see a big discrepancy between specified and measured values. This is mainly due to noise-margin and production tolerances for IC's.

It is of less importance how many gates the pulse generator can drive in the HIGH state. As we have shown, the limiting factor is the current sink capability of the driving source in the LOW state.

4. 8. Delaying pulses I

Hazard pulse

In the pulse technique there is often a need for delaying a pulse during a certain period of time. In a gate network, a pulse may have two possible parallel paths, one of these consisting of more gates than the other one, see fig. 4.58.

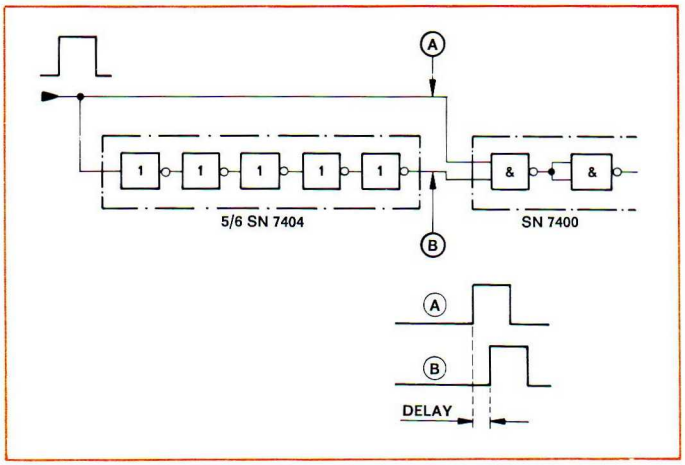


Fig. 4.58.

The internal time delay (t_d = propagation delay) of the gates may introduce a malfunction of the circuit. In figure 4.58, for example, an unintentional so-called hazard pulse may trigger a flip-flop or a counter and cause faults further in the circuitry, whose origin may be difficult to trace.

For SN 7404 the propagation delay t_d is 10 ns which in the set-up fig. 4.58 should provide a 50 ns hazard pulse.

Exercise 17

Verify existence of hazard pulse.

Equipment required:

1 pulse generator PM 5705 (PM 5704)
1 oscilloscope PM 3232
1 IC SN 7404 with datasheet
1 IC SN 7400 with datasheet
1 d.c. power supply +5 V (PM 5704 can be used)
1 resistor 50 ohm

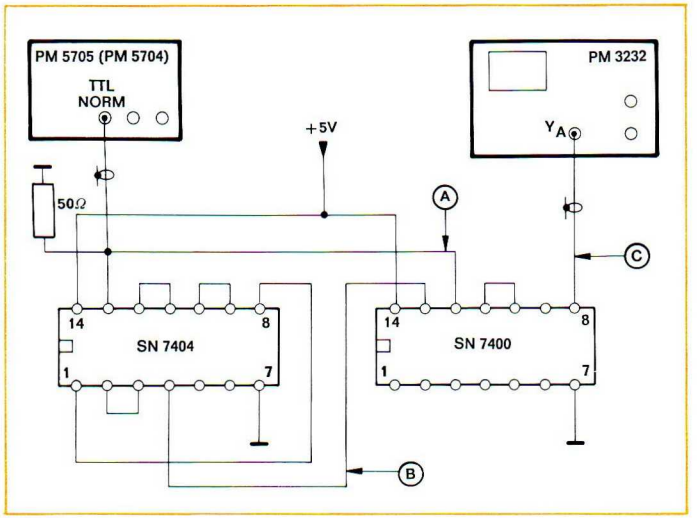


Fig. 4.59. Test set-up

Set the pulse generator:		Set the oscilloscope:	
DURATION	300 ns	TIME/cm	40 ns
REP.TIME	1 μs	AMPL. A	2 V/cm

Connect the TTL output of the pulse generator to the IC's as shown in the set-up diagram fig. 4.59. Connect the oscilloscope to points A, B, and C in the diagram.

Fig. 4.60. shows a typical measurement result.

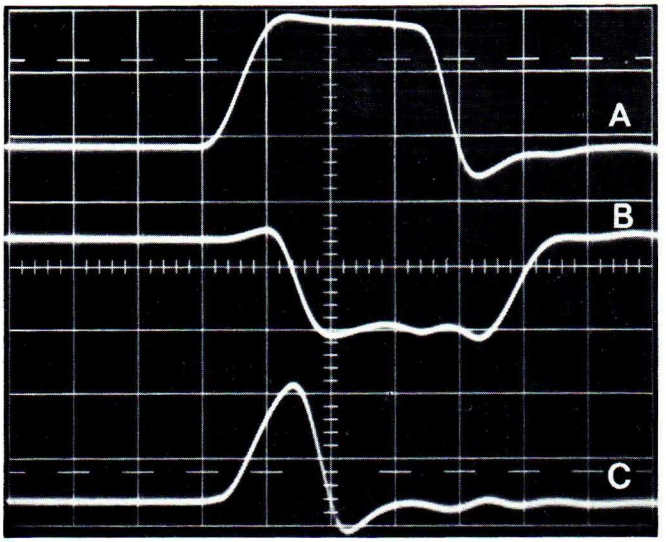


Fig. 4.60.

A. input pulse TTL
B. Delayed pulse
C. Hazard pulse approx 45 ns = delay in 5 inverters

4. 9. Delaying pulses II

Known delay using RC network

With the purpose to eliminate malfunctions due to propagation delays in gates and to ensure that the pulses arrive in the proper sequence, one can introduce known delays in the suitable signal paths.

The simplest delay is achieved by connecting an RC network between two gates, as shown in the following exercise.

Exercise 18

Equipment required:

1 pulse generator PM 5705 (PM 5704)
1 oscilloscope PM 3232
1 IC SN 7404 with datasheet
1 resistor 100 ohm
1 resistor 50 ohm
1 capacitor 220 nF
1 d.c. power supply +5 V (PM 5704 can be used)

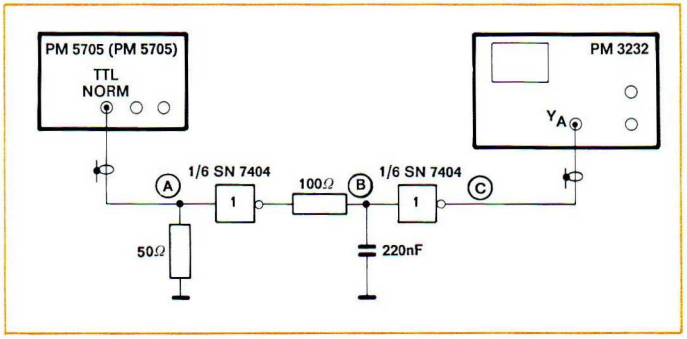


Fig. 4.61. Test set-up

Set the pulse generator:		Set the oscilloscope:	
REP.TIME	600 μs	TIME/cm	100 μs
SQUARE WAVE	depressed	AMPL.	2 V/cm

If the oscilloscope is connected progressively to points A, B and C, the diagram fig. 4.62. is obtained. See also fig. 4.63.

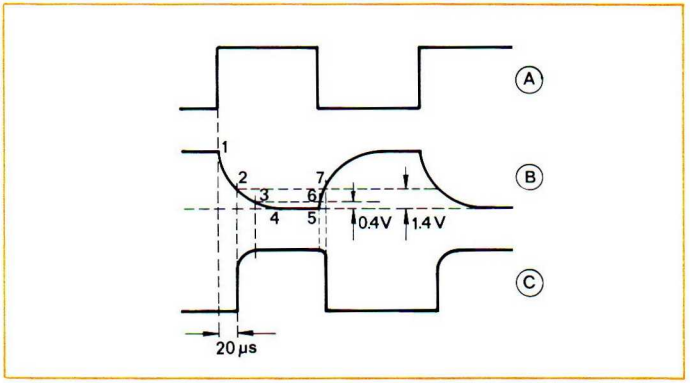


Fig. 4.62.

It appears from figure 4.62. that the edges of the delayed pulse C are non-linear. This, however, can be improved by connecting additional inverters.

Moreover, the trailing edge is more delayed than the leading edge, which makes that the duty factor of the delayed signal is changed. The delay of the trailing edge can be reduced by decreasing the value of capacitor C. However, the delay cannot be increased significantly with this set-up because the edge (the RC charging) which is triggering inverter 2 is too flack. This implies a risk for self-oscillation in the transition region.

The practical value of this set-up as a delay network is limited, but it provides an example of many of the parameters characterizing the TTL family.

An analysis of the waveform gives the following result (refer to the numbers of the waveform portions in figure 4.62. waveform B).

Portion 1—2
The delay of the leading edge is about 20 μs. The capacitor is discharged through R = 100 ohm plus the output impedance of inverter 1. A TTL output at LOW level has an impedance R_{out} of 12 ohm which is much lower than the R = 100 ohm used in this set-up. The time constant is $\tau = (R+R_{out})\ C$, which gives $\tau = 100+12)\ 0.22 \times 10^{-6} \approx 24$ μs. To increase the delay of the leading edge, resistor R can in our case be increased to maximum 250 ohm according to the relation $R \times I_{IL} < 0.4$ V, in which we assume $I_{IL} = 1.6$ mA.

Portion 2—3

The input voltage to inverter 2 reaches the threshold voltage $V_{th} = 1.3$ V and the transition is initiated. At point 3 the input voltage equals V_{OL} (output LOW) = 0.4 V which gives a maximum HIGH level for the next inverter.

In the first fraction of portion 2—3 the transistors are in their linear region, i.e. they act as common amplifiers. This region should be passed as fast as possible to avoid self-oscillation caused by capacitive feedback in the circuit.

Portion 6—7

The transition starts when the input voltage is 0.4 V. At this level the transistors become gradually less saturated until the input voltage is about 1 V. Now the inverter is in its linear region until the input voltage is 1.3 V where the transition is completed.

We can estimate the time constant τ to about 55 μs. Since $\tau = (R+R_{out})\,C$, we can calculate R_{out} to be about 150 ohm, which approximately equals the collector resistor of 130 ohm indicated in the circuit diagram of SN 7404 (refer to the data sheet).

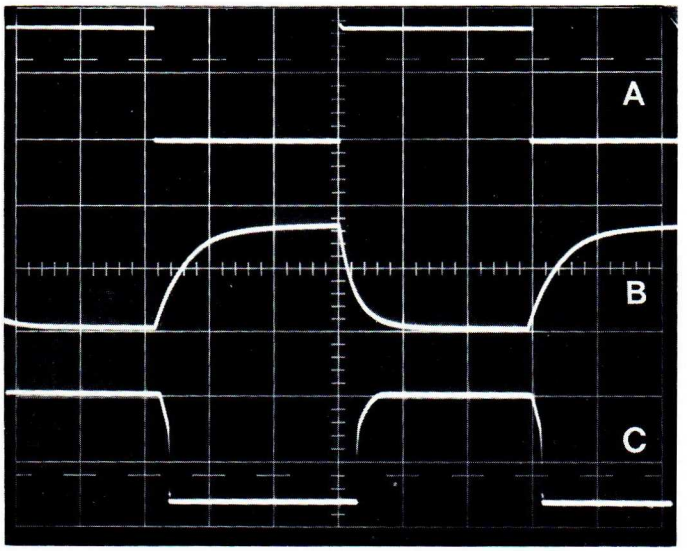


Fig. 4.63.
A. Input pulse TTL 2 V/cm
B. Capacitor voltage 1 V/cm
C. Delayed pulse 2 V/cm

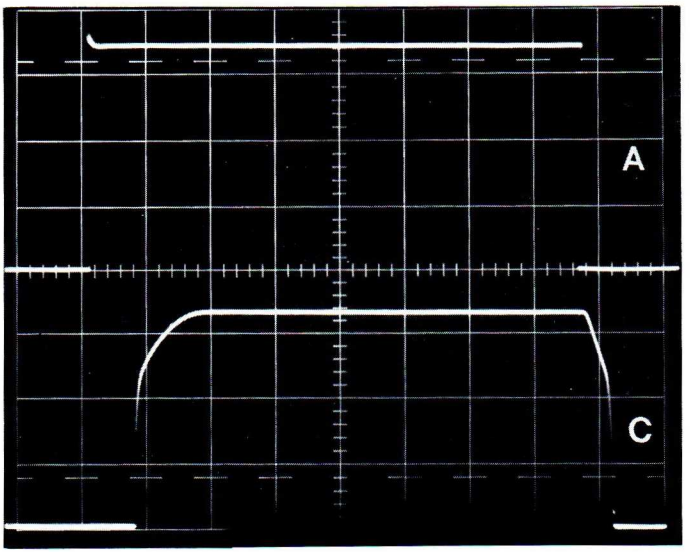


Fig. 4.64.
Close-up 50 μs/cm
A. 1 V/cm
C. 1 V/cm

4. 10. Delaying pulses III

Known delay using one-shots

There are many different varieties of pulse delays having more or less complicated set-ups. A simple circuit is achieved with two monostable multivibrators and a few gates as illustrated in figure 4.65.

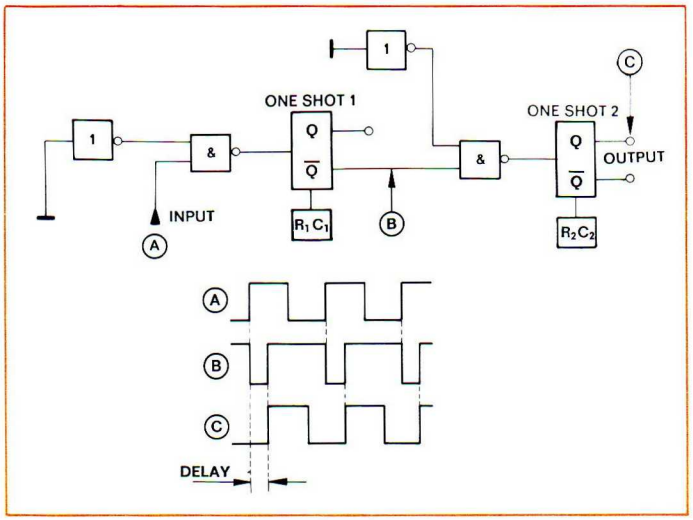


Fig. 4.65.

The gates are actually redundant because the one-shots are triggered on the positive edge, which means that the Q-output of one-shot 1 can be connected directly to the input of one-shot 2. However, exactly this configuration is contained in one single TTL package, the SN 74123. The duration of the mono-pulse is determined by the choice of the external R and C and can be varied between 45 ns and infinity.

The delay is set with one-shot 1 and will be approximately 0.35 R_1C_1 and the duration of the output pulse will be about 0.35 R_2C_2.

The factor 0.35 originates from the threshold voltage and swing of the TTL circuit.

There is, however, a major drawback with this method, viz. the input and output signals have the same duty factor only for one particular frequency unless R_2C_2 are changed.

Exercise 19

Equipment required:

1 pulse generator PM 5705 (PM 5704)
1 oscilloscope PM 3232
1 IC SN 74123 with datasheet
1 d.c. power supply (PM 5704 can be used)
2 resistors 22 kohm ≐ R1, R2
1 resistor 50 ohm
1 capacitor 10 nF = C1
1 capacitor 33 nF = C2

Set the pulse generator:		Set the oscilloscope:	
REP.TIME	500 μs	TIME/cm	100 μs
DURATION	200 μs	EXT. TRIGG	+

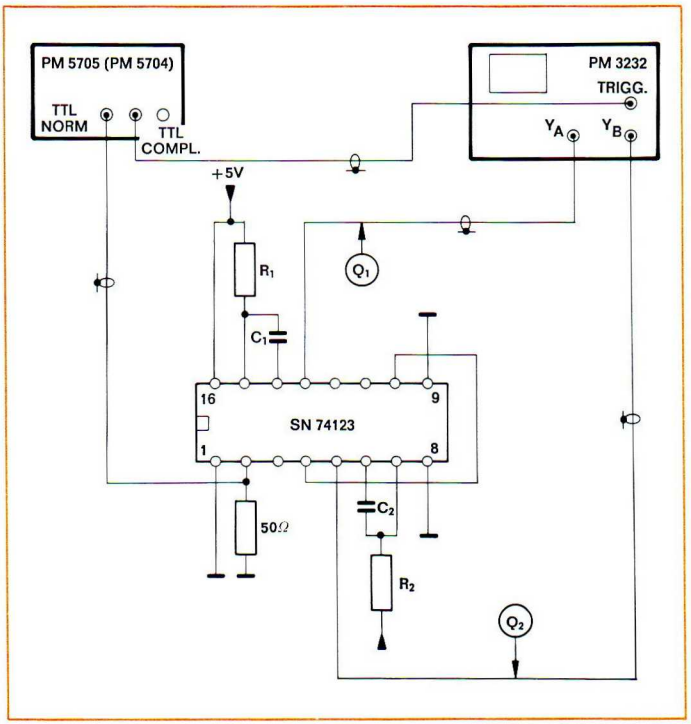


Fig. 4.66. Test set-up

Measure delay and duration and compare with the calculated values.

With R1 = 22 kohm, C1 = 10 nF, the delay will be about 0.35 x 220 = 75 μs.

If R2 = 22 kohm, C2 = 33 nF, the duration of the output signal will be 0.35 x 700 = 250 μs.

Notice that the pulse duration for Q_1 and Q_2 are independent of the pulse duration of the input signal. See fig. 4.67.

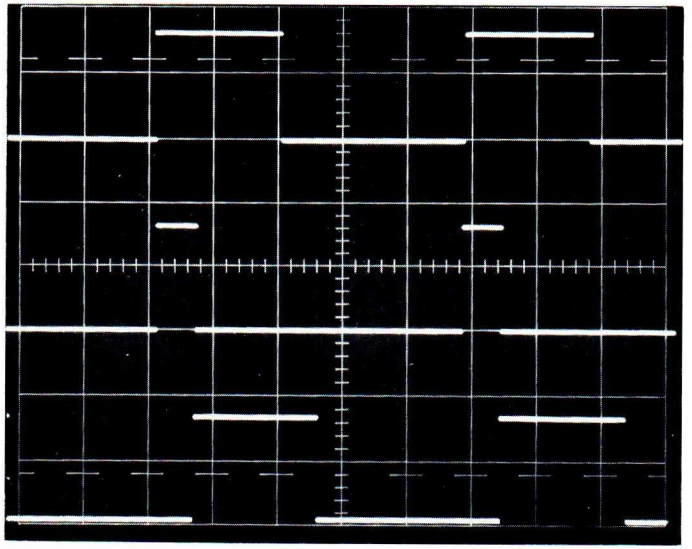


Fig. 4.67. Upper trace: Input signal
Middle trace: Q_1, delay is proportional to $R_1 \times C_1$
Lower trace: Q_2, output signal, duration is proportional to $R_2 \times C_2$

4. 11. TTL flip-flops and counters I

Ripple 4-bit counter

The JK Master-Slave flip-flop is the most frequently used memory device in the TTL family.

In the 74 series, the flip-flop is available in a great number of packages having different configurations. By connecting the data and trigger inputs in different ways, one can obtain a virtually unlimited variation of the function.

As an example we may select the SN 7476N containing two JK flip-flops (see fig. 4.68.).

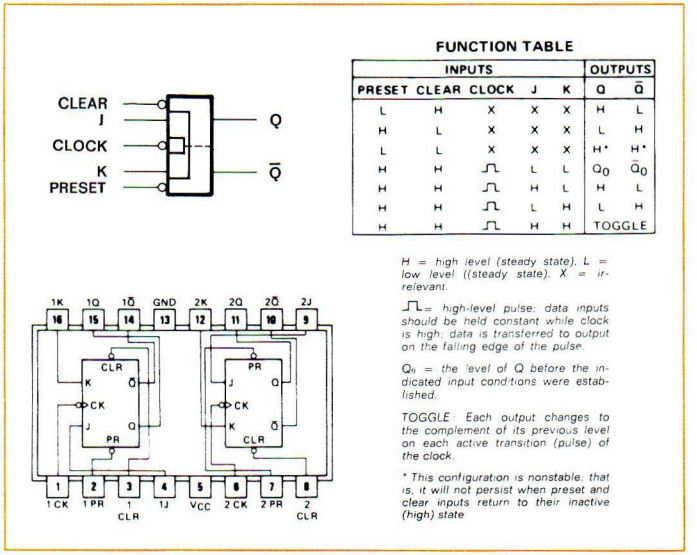


Fig. 4.68. Schematic symbol, truth table and data sheet drawing of SN 7476N

The data from the JK inputs are stored in the flip-flop when the clock pulse occurs and will be available at the Q output when the clock pulse ceases (Master-Slave flip-flop).

The "Clear" input sets Q = 0 and the "Preset" input sets Q = 1 when they are connected to LOW level. These inputs are independent of the clock pulse.

If the JK inputs are connected to $\overline{Q}$ and Q respectively the flip-flop will change its state after each clock pulse and the frequency of the output signal will be half of the frequency of the input signal (see fig. 4.69.).

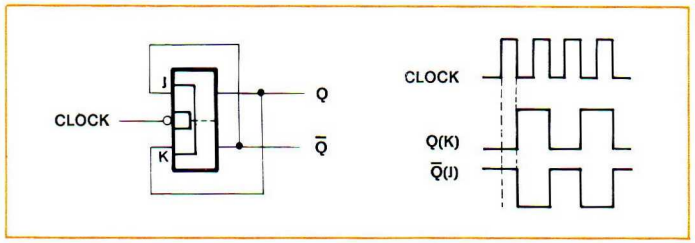


Fig. 4.69.

If four JK flip-flops are cascade connected, i.e. the clock input is connected to the Q output of the foregoing flip-flop, a ripple binary counter is obtained which can count to 16 (see fig. 4.70).

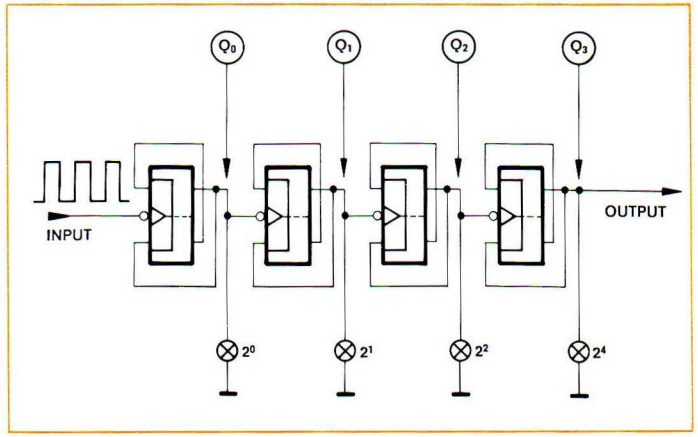


Fig. 4.70.

The result can be read in binary form if a lamp or a light-emitting diode is connected to each Q output. At every 16th pulse, all lamps will be off and the counting cycle starts again.

Exercise 20

Equipment required:

1 pulse generator PM 5705 (PM 5704)
1 oscilloscope PM 3232
2 IC's SN 7476 with datasheet
4 resistors 100 ohm
1 resistor 50 ohm
4 light-emitting diodes
1 d.c. power supply +5 V (PM 5704 can be used)
1 BNC T-piece

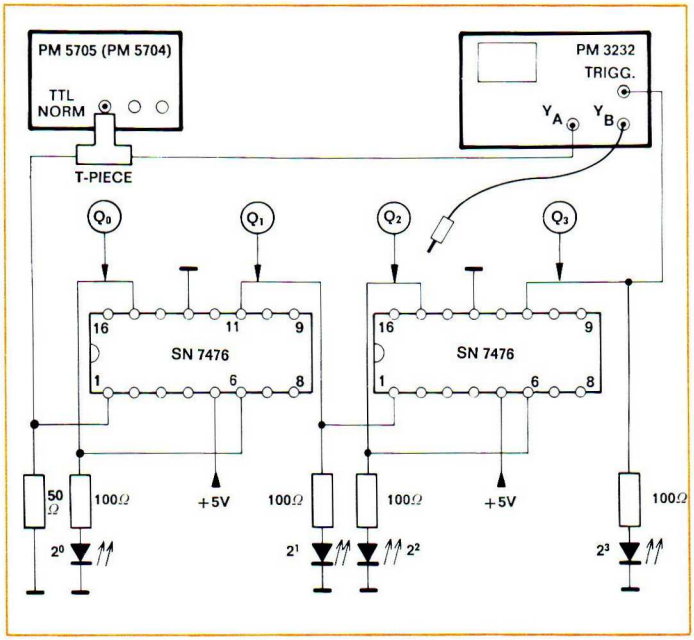


Fig. 4.71. Test set-up

Connect the flip-flops with the aid of the datasheet and the diagram fig. 4.71. First set the pulse generator to EXT+ and generate pulses manually to check the function of the set-up by depressing the button SINGLE SHOT.

Set the rep.time to 10 μs and connect the oscilloscope to the input signal and the outputs of the flip-flops in sequence. Trigger the oscilloscope externally as shown in the set-up diagram fig. 4.71.

The time base of the oscilloscope is set in such a way that precisely 16 pulses cover the screen. See fig. 4.72.

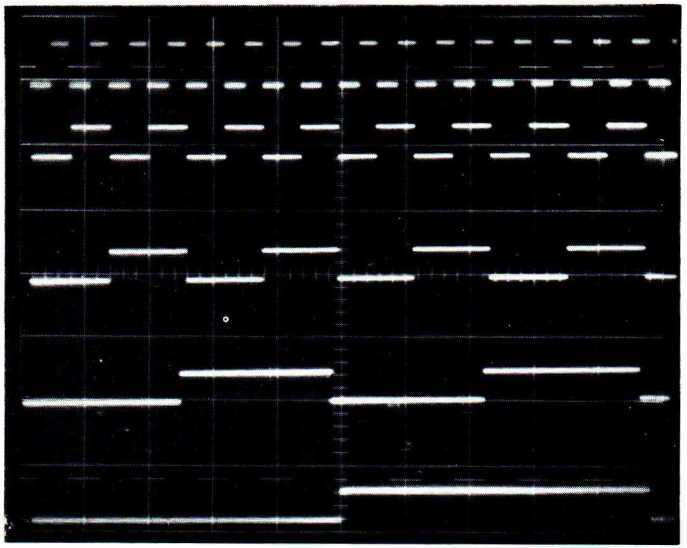


Fig. 4.72. 5 V/cm, 10 μs/cm, uncalibrated. Upper trace: A input signal.
Remaining traces (from top) channel B, Q_0, Q_1, Q_2, Q_3.

Note that the counting result is 1000 after the 8th pulse. Compare with the result obtained in exercise 21.

4.12. TTL flip-flops and counters II

Ripple decade counter

There is a frequent need for a counting cycle which has not the radix 2 ($16 = 2^4$), for example, 10 in a decade system. This can be achieved by forcing the flip-flops to leave out 6 states in a binary counter employing 4 flip-flops. After 7 pulses the state is 0111. Assuming that the 8th pulse would give the result 1110 instead of 1000, pulses 9 and 10 would give 1111 and 0000 respectively at the Q outputs.

The discontinuity after pulse 7 can be accomplished by setting Q_1 and Q_2 to "1" via their preset inputs. These inputs require a logical "0" during at least 20 ns, and this pulse can be achieved by means of Q_3 which is set to "1" after pulse 8. See fig. 4.73.

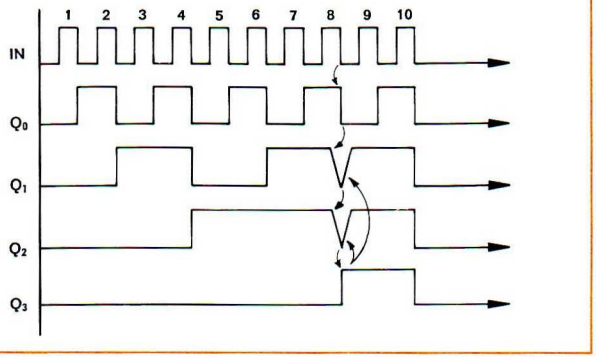


Fig. 4.73. Timing diagram for a ripple decade counter

The preset pulse is achieved in a simple way by a delay caused by a few inverters (refer to section 4.8. Delaying pulse I). See fig. 4.74.

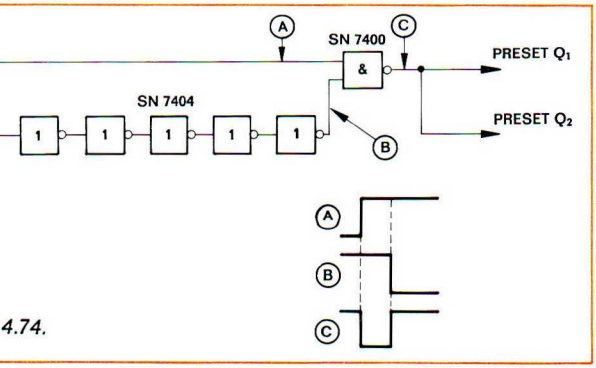


Fig. 4.74.

Exercise 21

Use the same equipment and set-up as in exercise 20, but add one SN 7404 and one SN 7400.

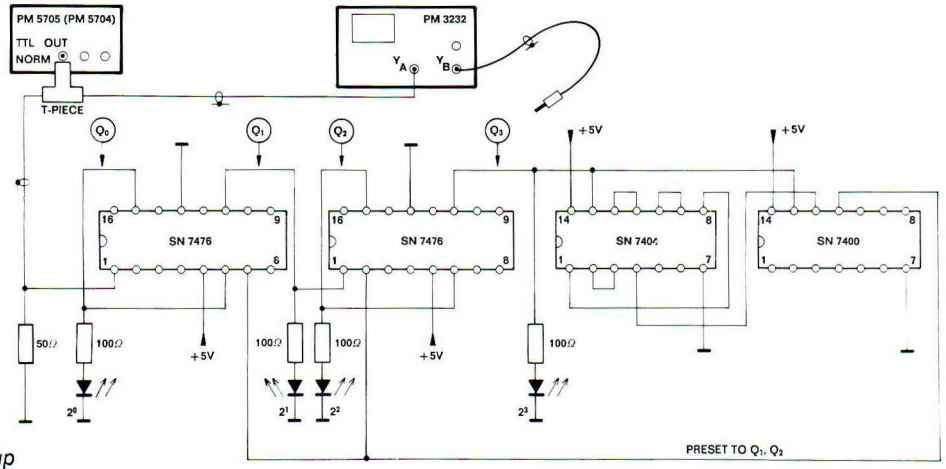


Fig. 4.75. Test set-up

The pulse generator is connected as in exercise 20. Using the SINGLE SHOT function, we can verify that the counter now has a cycle of 10 pulses.

The result read on the lamps or LED's however, does not correspond anymore to the number of counted pulses in the binary form.

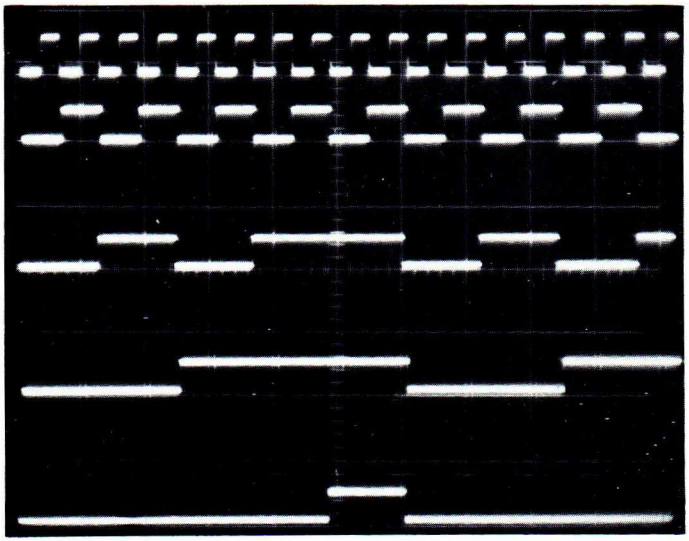


Fig. 4.76. 10 µs/cm uncalibrated. Upper trace, ch. A, input signal
Lower traces, ch. B (from top): Q_0, Q_1, Q_2, Q_3
Note that Q_1 and Q_2 are set to "1" after the 8th pulse

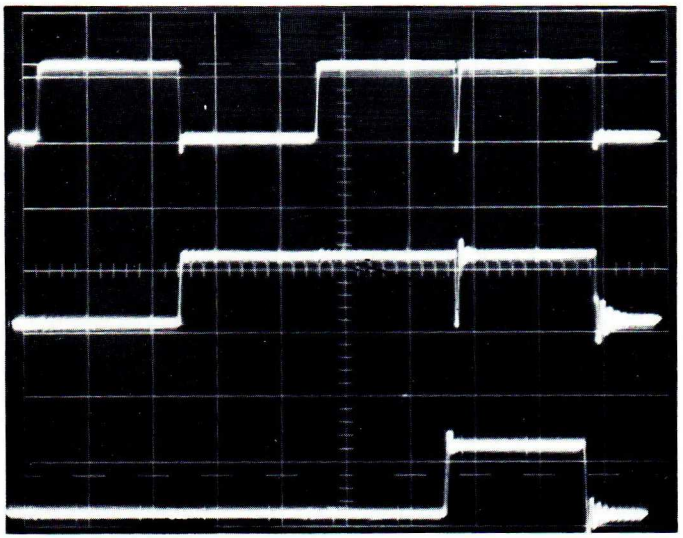


Fig. 4.77. Close-up of the "preset" event. PM 5705: Rep time 1 µs
PM 3232: 1 µs/cm, calibrated
Traces from top: Q_1, Q_2, Q_3.

4.13. TTL flip-flops and counters III

Modified ripple counter

Very often it is desirable to have the result of a decade counter directly in binary form, i.e. pulses 8, 9 and 10 should be presented as 1000, 1001, and 0000 respectively. The ripple decade counter can be modified to such a binary counter by inhibiting the sequence after 10 pulses, e.g. by means of a "Clear" pulse to all flip-flops.

Exercise 22

Use the same equipment as in exercise 20, but add a NAND gate (SN 7400) as illustrated in the test set-up diagram fig. 4.78.

Set the pulse generator:

REP.TIME 1 μs
SQUARE WAVE depressed

Set the oscilloscope:

TIME/cm 1 μs

The "Clear" pulse is obtained from a NAND gate whose inputs are controlled by outputs Q_1 and Q_3. After pulse 10, these outputs are set to "1" and the gate provides a "0" to the flip-flops. Q_1 and Q_3 go "1" again, the NAND gate provides a "1" to the flip-flops, and the cycle is repeated.

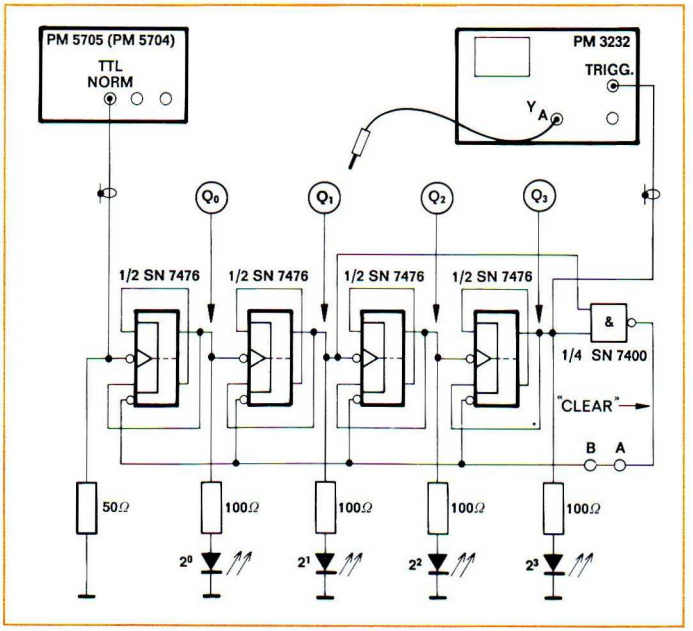


Fig. 4.78. Test set-up

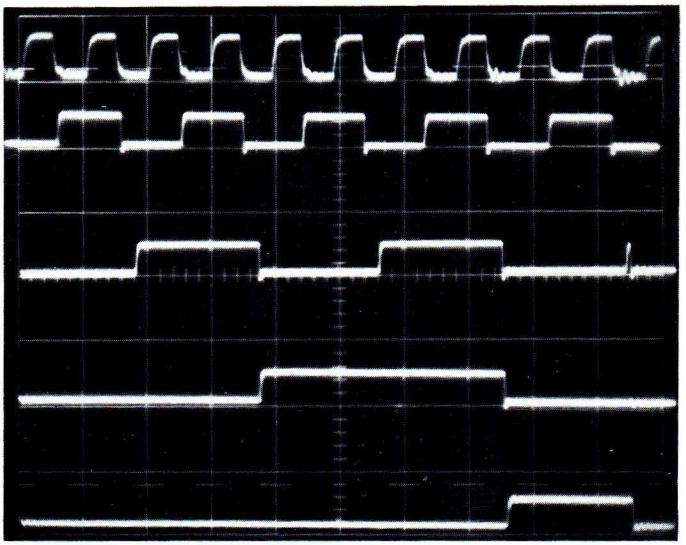


Fig. 4.79. Upper trace: input signal
Lower traces (from top): Q_0, Q_1, Q_2, Q_3
Note that Q_3 first goes to "1" before the "Clear" pulse can set all flip-flops to "0".

There are two major drawbacks with the circuit described above:

1. There is a spike pulse occurring at the Q_1 output when the flip-flops are set to zero after each cycle.
2. There is some uncertainty in the function because of different time delay between the Clear input and the Q output in the various flip-flops.

If, for example, Q_3 has a longer time delay than Q_1, the Q_1 may switch over to LOW output before Q_3. The NAND gate and the Clear signal will then go HIGH causing that Q_3 will not switch over before the next cycle starts.

This problem can, however, be solved by introducing a latch flip-flops between point A and B in figure 4.78.
A suitable circuit for this purpose is SN 7400, see fig. 4.80.

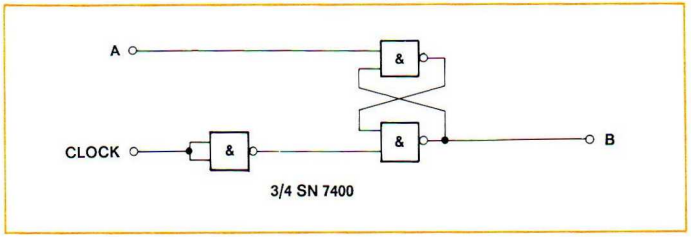


Fig. 4.80.

The spikes at the output of Q_1 can be eliminated by using another type of counter, e.g. a synchronous counter, which is described in section 4.14.

4.14. TTL flip-flops and counters IV

Synchronous counter

The major characteristic of a synchronous counter is that all inputs are triggered simultaneously, and the transition condition is determined by the logical level at the data input J and K. From the truth table of the JK flip-flop it appears that the state 11 initiates a transition, but the 00 state does not involve any change of the output levels.

Exercise 23

Equipment required:

1 pulse generator PM 5705 (PM 5704)
1 oscilloscope PM 3232
2 IC SN 7476 with datasheet
1 IC SN 7400 with datasheet
1 IC SN 7410 with datasheet
1 d.c. power supply +5 V (PM 5704 can be used)
1 resistor 50 ohm
1 resistor 7,5 kohm

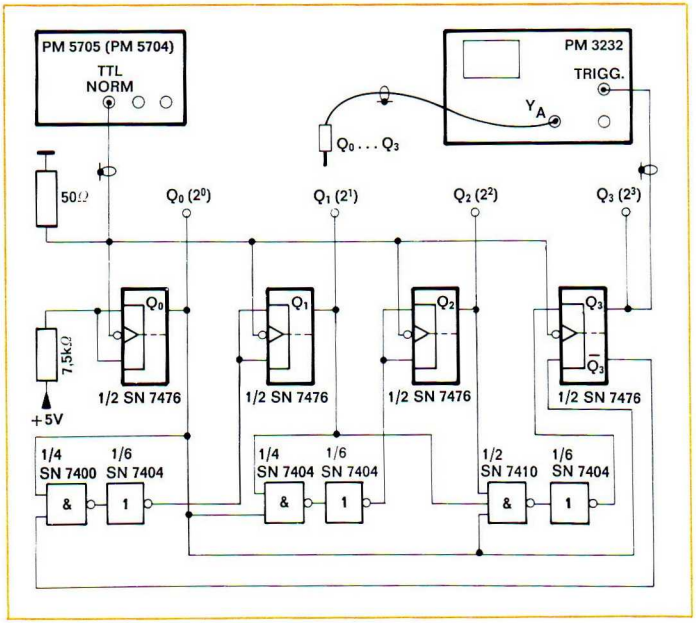


Fig. 4.81. Test set-up

Set the pulse generator:		Set the oscilloscope:	
REP.TIME	15 μs	TIME/cm	20 μs
DURATION	50 ns	EXT. TRIGG	—

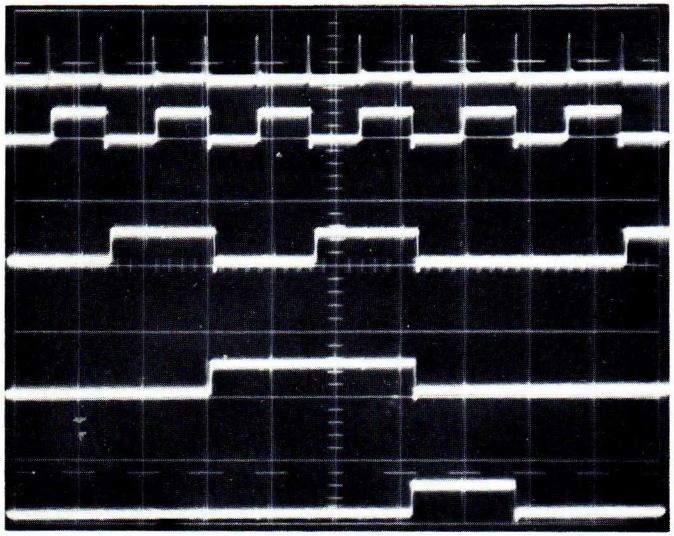
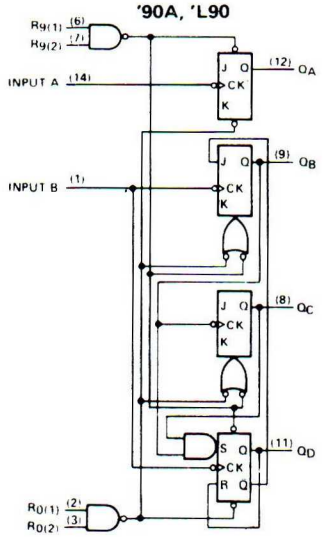


Fig. 4.82. *Upper trace: input signal*
Lower traces (from top): Q_0, Q_1, Q_2, Q_3.

Decade counters employing the BCD code are available in several executions in the 74 series, for example the SN 7490 (see fig. 4.83.).

This counter can handle frequencies exceeding 10 MHz. The minimum pulse duration is specified to 50 ns which can be verified by using the PM 5705 (PM 5704).



'90A, 'L90
BCD COUNT SEQUENCE
(See Note A)

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

'90A, 'L90
RESET/COUNT FUNCTION TABLE

RESET INPUTS				OUTPUT			
$R_{0(1)}$	$R_{0(2)}$	$R_{9(1)}$	$R_{9(2)}$	Q_D	Q_C	Q_B	Q_A
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L	COUNT			
L	X	L	X	COUNT			
L	X	X	L	COUNT			
X	L	L	X	COUNT			

NOTE : A. Output Q_A is connected to input B for BCD count.

Fig. 4.83. *Truth tables, diagram of SN 7490*

Exercise 24

Equipment required:

1 pulse generator PM 5705 (PM 5704)
1 oscilloscope PM 3232
1 IC SN 7490 with datasheet
1 resistor 50 ohm
4 resistors 100 ohm
4 light-emitting diodes
1 d.c. power supply +5 V (PM 5704 can be used)

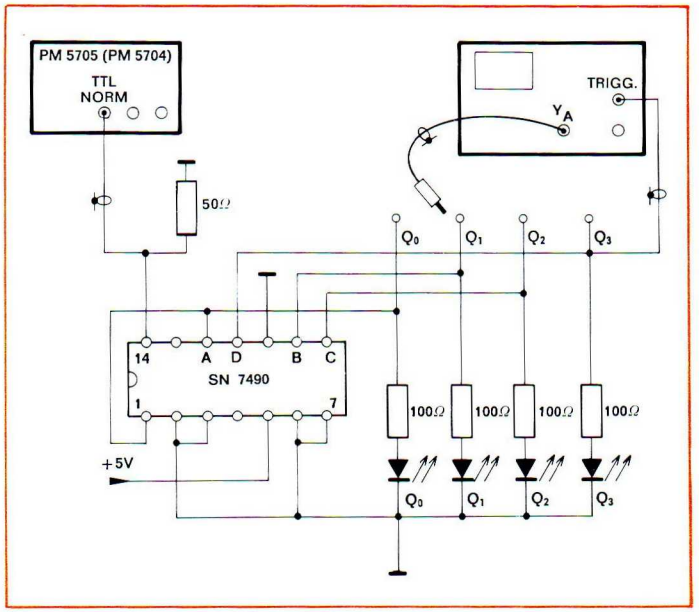


Fig. 4.84. Test set-up

Set the pulse generator:		Set the oscilloscope:	
REP.TIME	15 μs	TIME/cm	20 μs
DURATION	100 ns	AMPL. A	5 V/cm
		EXT. TRIGG	—

Connect the oscilloscope to Q_0.

Decrease the pulse duration successively and note if the SN 7490 stops counting below 50 ns.

4.15. CMOS vs TTL: power consumption

CMOS circuits are characterized by a very low power consumption which is dependent of the supply voltage, the magnitude of the capacitive load and how often the gate is changing its state, i.e. the pulse frequency.

Exercise 25

Equipment required:

1 pulse generator PM 5705
1 oscilloscope PM 3232
1 d.c. power supply +5 V to +15 V
1 DC/AC amp.meter 50 μA
1 IC CD 4011A with datasheet
1 IC SN 7400 with datasheet
1 resistor 50 ohm
4 capacitors 15 pF = C_L
1 capacitor 2.2 μF

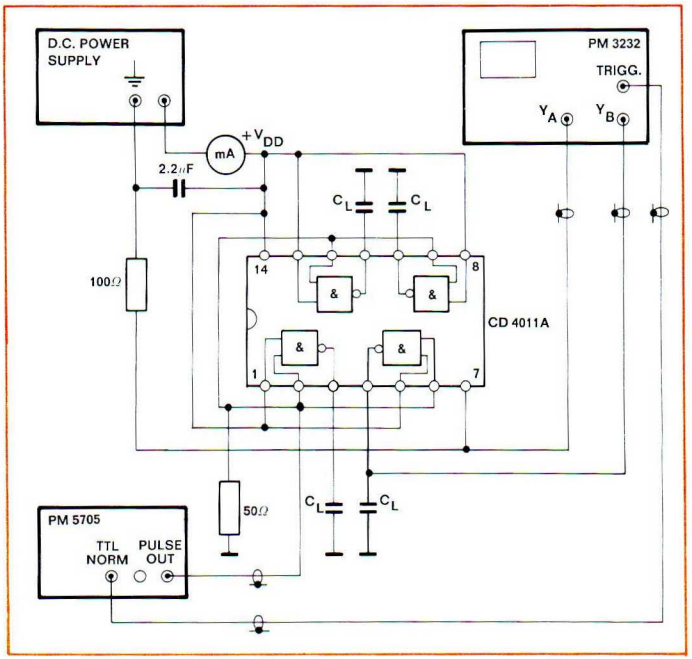


Fig. 4.85. Test set-up

WARNING:

The amplitude of the pulse generator may not exceed the supply voltage of +10 V! Otherwise the CMOS circuit may be damaged.

Set the pulse generator:		Set the oscilloscope:	
REP.TIME	10 μs	TIME/cm	2 μs
DURATION	5 μs		
AMPL.	max. 10 V		

The current from the power supply is measured with a common DC/AC amp.meter having a sensitivity down to about 50 μA at full deflection. The ampmeter will show an approximate mean value of the current, which is, however, sufficient for indicating the differences between TTL and CMOS. The current shape can be observed on the oscilloscope if a 100 ohm resistor is connected as shown in the diagram fig. 4.85.

The oscillogram fig. 4.86. shows a typical measurement result.

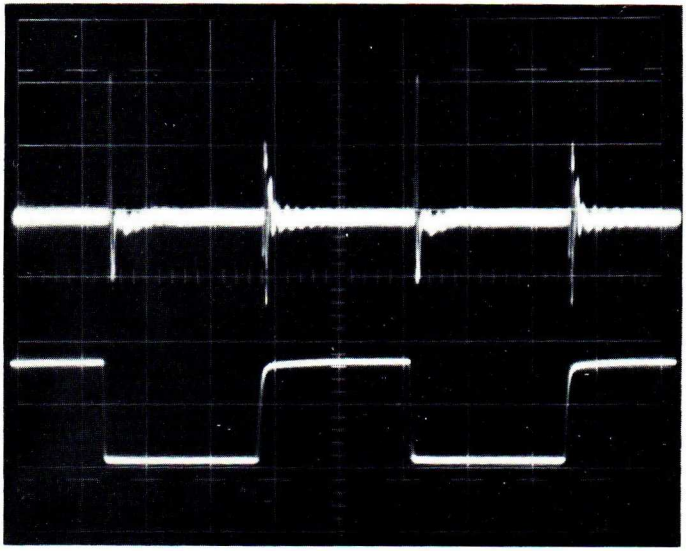


Fig. 4.85. Upper trace (A): voltage across the 100 ohm resistor
200 mV/cm 2 μs/cm
V_{DD} = 10 V
Lower trace (B): CMOS pulse
5 V/cm 2 μs/cm

If the current through the amp.meter is measured both for a logical "1' and a logical "0" at the output, and in addition, for some different frequencies and supply voltages, an estimation of the power consumption of the CMOS circuit can be made.

CMOS (4 NAND gates)

		EXT. + Norm. Compl.		REP.TIME (Duration = 0.5 x REP.TIME)			
V_{DD}	PM 5705 AMPL.	"0"	"1"	1 ms (1 kHz)	100 μs (10 kHz)	10 μs (100 kHz	1 μs (1 MHz)
5 V	4 V	0	$<$0.5 μA	3	9	70	700 μA
10 V	9 V	0	$<$0.5 μA	5	9	100	1100 μA
15 V	14 V	0	$<$0.5 μA	10	20	130	2500 μA

Note:
When measuring at logical "0" and "1", set the pulse generator to EXT.+ and set the main output to NORMAL and COMPL. respectively.
Calculate the power consumption for each value of V_{DD}!

Exercise 26

Use the same equipment as in exercise 25, but replace the CMOS circuit by a TTL circuit SN 7400 and the 100 ohm resistor at the power supply by a 10 ohm resistor. Note that a PM 5704 can be used instead of the power supply.

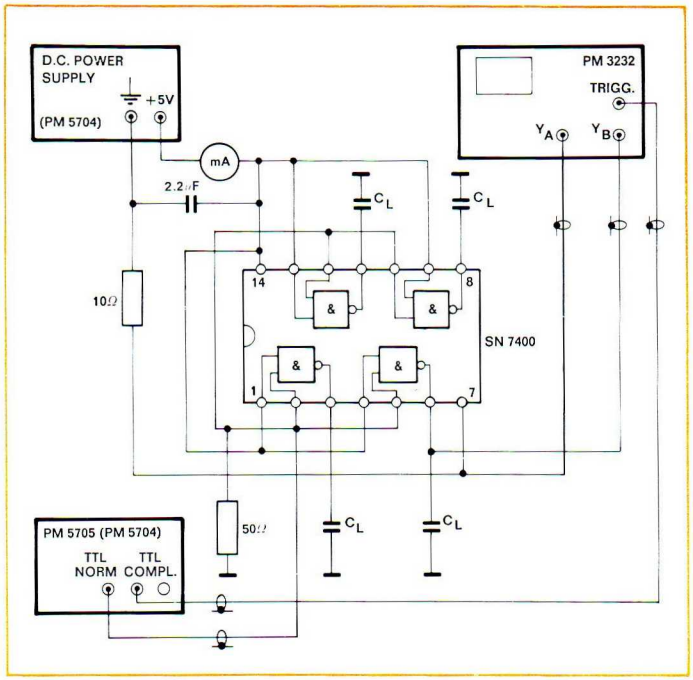


Fig. 4.87. Test set-up

Measure the current consumption as in exercise 25:
TTL (4 NAND gates)

V_{CC}	PM 5705 (PM 5704)	EXT. +		REP.TIME (Duration = 0.5 x REP.TIME)			
		Norm.	Compl.				
		"0"	"1"	1 ms (1 kHz)	100 μs (10 kHz)	10 μs (100 kHz)	1 μs (1 MHz)
5 V	TTL Out	17	5	11	11.5	11.6	14 mA

Note:

When measuring at logical "0" and "1", set the pulse generator to EXT.+ and connect the TTL OUT NORMAL and COMPL. respectively to the SN 7400.

Calculate the power consumption and compare with the calculated consumption of the two CMOS gates!

4.16. CMOS vs TTL: speed

To compare the speed between CMOS and TTL circuits one can measure the rise and fall times of two gate networks with identical configuration.
CD 4011A and SN 7400 each contain four dual input NAND gates.

Exercise 27

Equipment required:

1 pulse generator PM 5705
1 oscilloscope PM 3232
1 d.c. supply +10 V
1 IC CD 4011A with datasheet
1 IC SN 7400 with datasheet
1 coaxial cable, 50 ohm, length about 50 cm
1 BNC T-piece
1 resistor 50 ohm

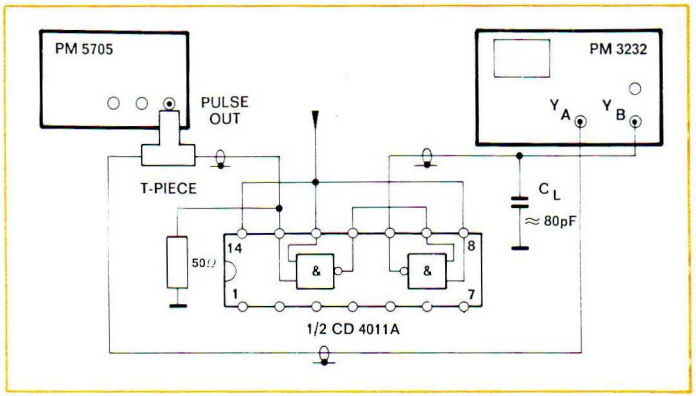


Fig. 4.88. Test set-up

The capacitive load C_L is a 50 cm piece of coaxial cable plus the inherent capacitance of the oscilloscope.

WARNING!

The amplitude of the pulse generator may not exceed the supply voltage V_{DD} ! Otherwise the CMOS circuit may be damaged.

Set the pulse generator:		Set the oscilloscope:	
REP.TIME	10 μs	TIME/cm	100 ns
DURATION	5 μs	AMPL. A	1.25 V/cm
AMPL.	10 V	AMPL. B	1.25 V/cm

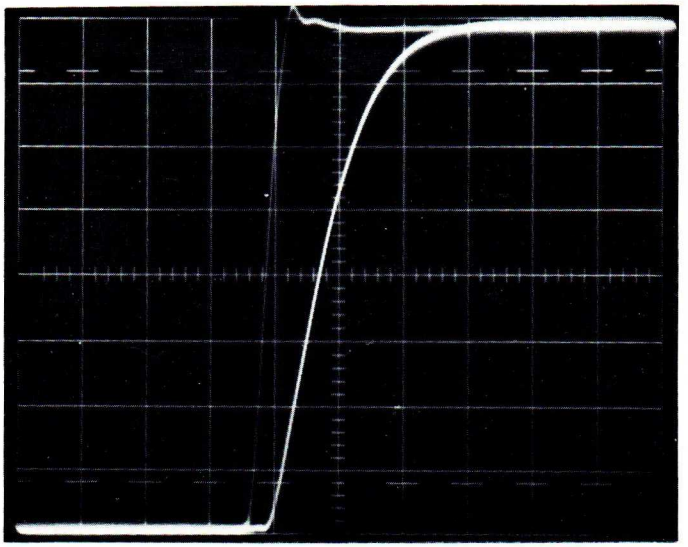


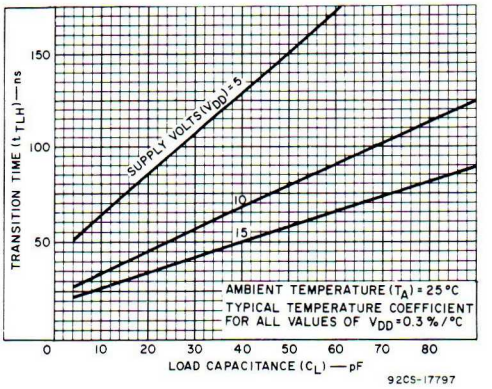
Fig. 4.89. Low-to-high transition

Fig. 4.89. illustrates the input and output signals at low to high transition.

The rise time is somewhat decreased if both inputs of the gates are driven in parallel.

The bold waveform represents the rise time of the CMOS circuit, which is about 150 ns.

Since the propagation time delay for 2 gates is approximately 80 ns, the propagation time delay LOW to HIGH, t_{PLH}, will be 40 ns.



Typ. low-to-high transition time vs. C_L.

Fig. 4.90. shows the input and output signals at high-to-low transition.

The bold waveform represents the fall time of the CMOS circuit which is about 150 ns. The propagation time delay t_{PHL}, can be calculated to 50 ns.

If the SN 7400N is used in the set-up instead of the CD 4011A, and is driven by the TTL output of the pulse generator, the times measured will be significantly shorter.

To make the measurement, connect all four gates of the IC in series and divide the measured propagation time delay by 4.

Typical values are for the rise and fall times 5 ns, and propagation time delay 10 ns.

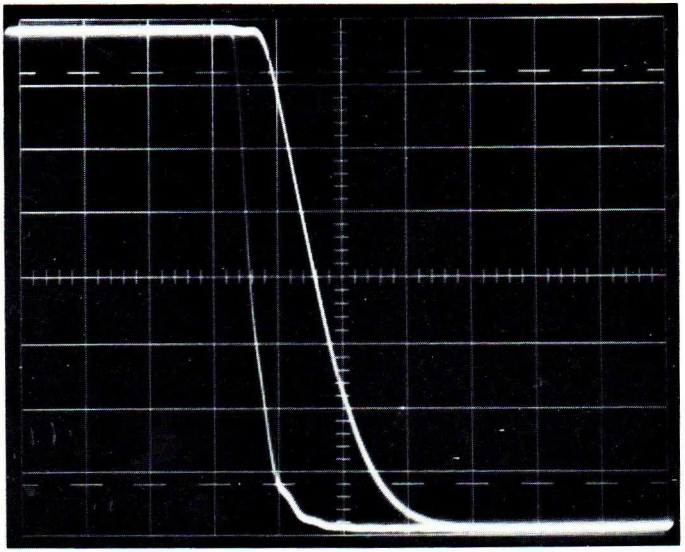
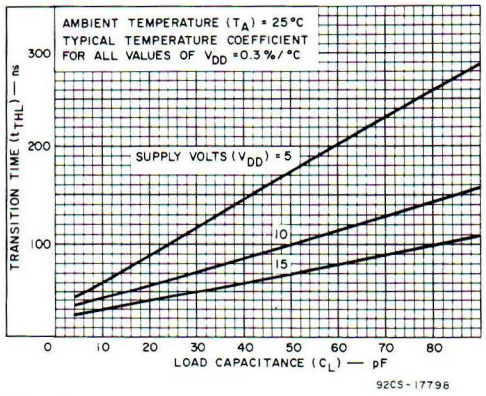


Fig. 4.90. High-to-low transition



Typ. high-to-low level transition time vs. C_L — CD4011A & CD4023A.

4.17. CMOS vs TTL: Supply voltage influence on rise time

TTL and CMOS exhibit a significant rise time difference if they are connected to the same supply voltage and are driven from the same signal source.

Exercise 28

Equipment required:

1 pulse generator PM 5705
1 oscilloscope PM 3232
1 DC power source +5 V
1 IC SN 7400 with datasheet
1 IC CD 4011A with datasheet
1 resistor 50 ohm
2 coaxial cables length 30 cm (forms load capacitance C_L together with inherent capacitance of oscilloscope).

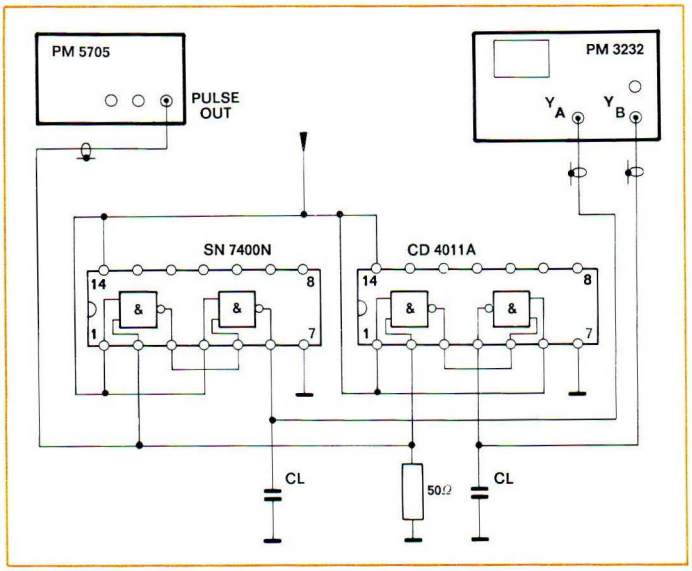


Fig. 4.91. Test set-up

WARNING!

The amplitude of the pulse generator may not exceed the supply voltage V_{DD} Otherwise the CMOS circuit may be damaged.

Set the pulse generator:		Set the oscilloscope:	
REP.TIME	10 μs	TIME/cm	1 μs
DURATION	5 μs	AMPL. A	2 V/cm
AMPL.	5 V	AMPL. B	2 V/cm
INT.LOAD	50 ohm		

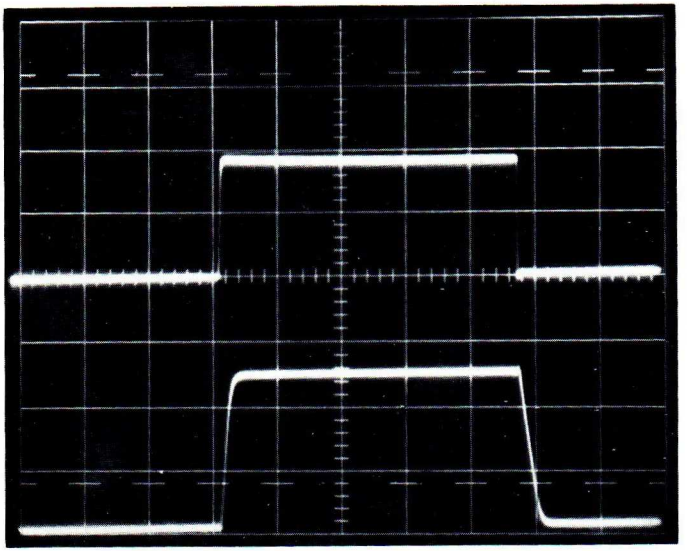


Fig. 4.92. Upper trace: Channel A, TTL pulse
Lower trace: Channel B, CMOS pulse

Fig. 4.92. shows the difference between the TTL and CMOS pulses.

This deviation of rise time is caused by the fact that the circuits have different output impedances, for TTL about 100 ohm and for CMOS as high as 1 kohm. The capacitance C_L which is permanently present at the output, forms together with the output impedance an RC network having a varying time constant. See fig. 4.93.

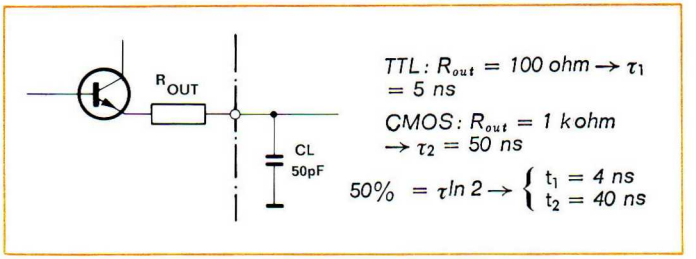


Fig. 4.93.

In the CMOS circuits, the output impedance is changed with the supply voltage. This phenomenon occurs because the conductivity of the conductor channel is increasing, i.e. the resistance is decreasing when the voltage V_{DS} is increasing. The current supposed to charge and discharge internal and external capacitance is increasing which implies a reduced time constant and a faster transition.

Exercise 29

Verify the relation between supply voltage and risetime of a CMOS circuit.

Use the same equipment as in exercise 28, but leave out the TTL circuit SN 7400.

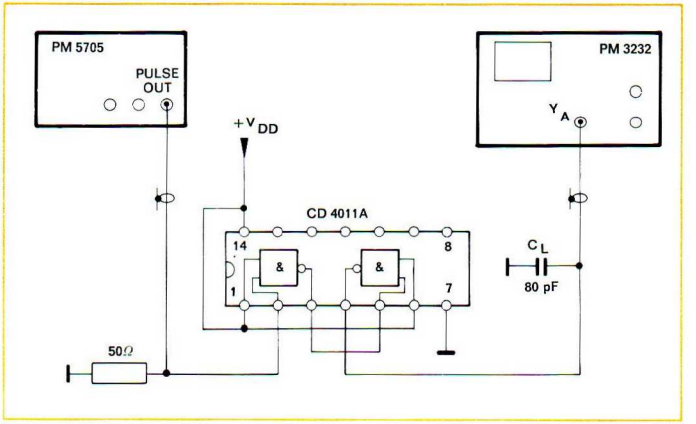


Fig. 4.94. Test set-up

Set the pulse generator:

REP.TIME	10 μs
DURATION	5 μs
AMPL.	5 V

Set the oscilloscope:

TIME/cm	100 ns

Change the supply voltage V_{DD} progressively to +5 V, +10 V and +15 V. Note that the CMOS circuits should be driven with the same voltage as the supply voltage.

Therefore, the amplitude of the generator's PULSE OUT should be changed simultaneously with V_{DD}. The transition level of CMOS equals approximately half the V_{DD}.

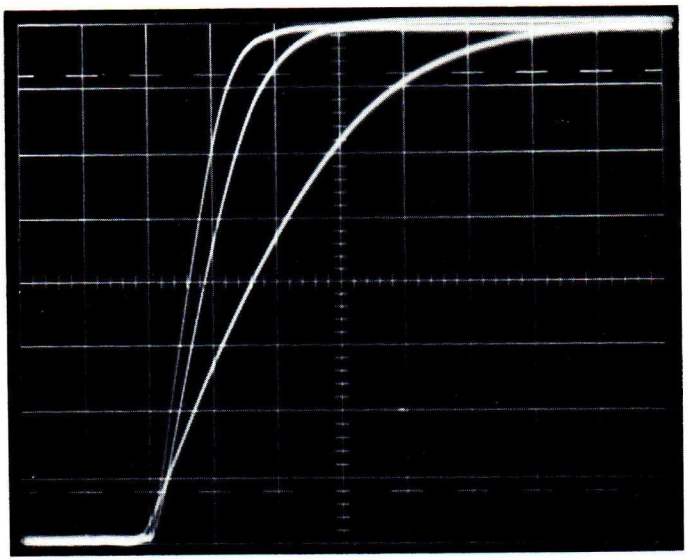


Fig. 4.95. CMOS risetime at 100 ns/cm

Refer to fig. 4.95. and read approximately the following rise times of the CMOS circuit (from left to right) at varying supply voltages:

V_{DD}	t_r
15 V	120 ns
10 V	180 ns
5 V	400 ns

4.18. CMOS analogue amplifier

In TTL circuits it is important that the transition level is passed with an edge which is as fast as possible. Otherwise self-oscillations may occur, caused by the input transistors which are in their linear region during the transition interval.

A fast passage of the transition level is also desirable for CMOS circuits in digital applications. CMOS, however, offers a possibility to use the MOS transistors included in the circuit as linear amplifiers by biasing the input with approximately half the supply voltage. See figure 4.96.

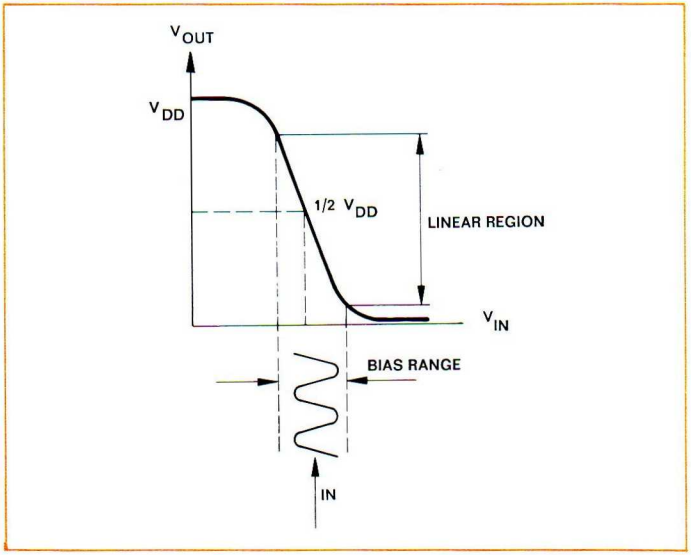


Fig. 4.96.

The bias can be adjusted in several ways. In general it is quite sufficient to place a resistor of 1 to 10 Mohm between input and output to reach a supply voltage of $0.5 \times V_{DD}$, see fig. 4.97.

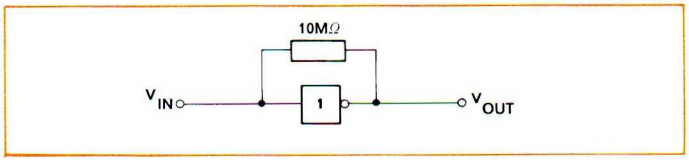


Fig. 4.97.

Fig. 4.98. shows another alternative; feed-back via a variable resistor R_1 and a resistor R_2 to ground. R_1 sets the working point to the desired level.
With this arrangement the amplifier has an inverting function and a gain of 10 to 30 times.

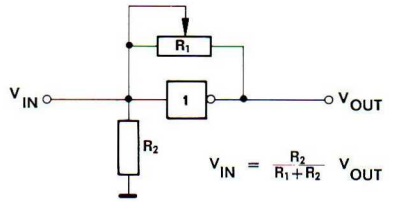


Fig. 4.98.

Exercise 30

Equipment required:

1 pulse generator PM 5705
1 oscilloscope PM 3232
1 CMOS circuit CD 4007A with datasheet
1 DC power supply + 10 V
1 resistor 100 kohm
1 resistor 10 Mohm
1 variable resistor 10 kohm
1 capacitor 1 μF

The circuit CD 4007A contains six MOS transistors, which can be interconnected to perform various functions, for example, three inverters.

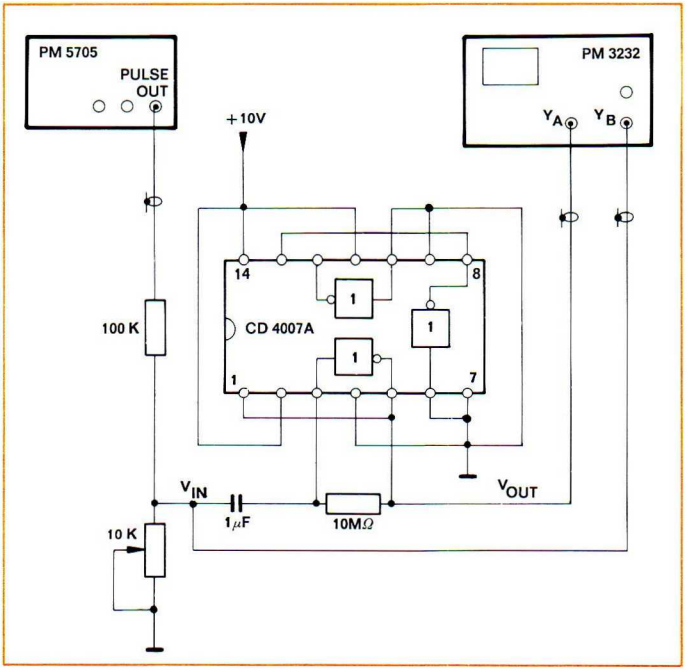


Fig. 4.99. Test set-up

Set the pulse generator:		Set the oscilloscope:	
REP.TIME	100 μs	TIME/cm	20 μs
DURATION	50 μs	AMPL. A	2 V/cm
		AMPL. B	0.2 V/cm

The working point will be adjusted to about 5 V. The input voltage V_{in} is adjusted partly with the pulse generator's amplitude control, partly with the variable resistor 10 K. Fig. 4.100. shows a typical measurements result.

The gain can be calculated to 15 times.

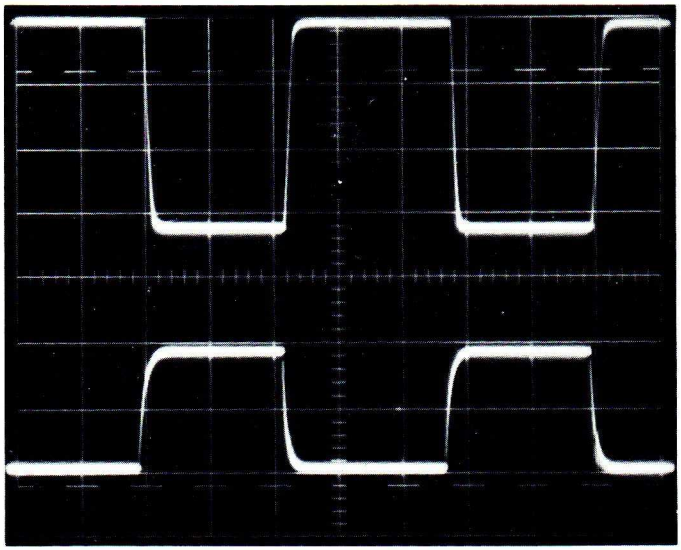


Fig. 4.100. Upper trace: channel A, 2 V/cm. Amplitude 6 V_{p-p}
Lower trace: channel B, 0.2 V/cm
Amplitude of V_{in} 0.4 V_{p-p}

4.19. CMOS Schmitt trigger

A Schmitt trigger is used to convert slow edges into distinct pulses, for instance, in trigger circuits.

To eliminate noise and interference on the input signal the Schmitt trigger has different threshold levels for increasing and decreasing input signal. In other words, there is a certain hysteresis in the transfer functions. See fig. 4.101.

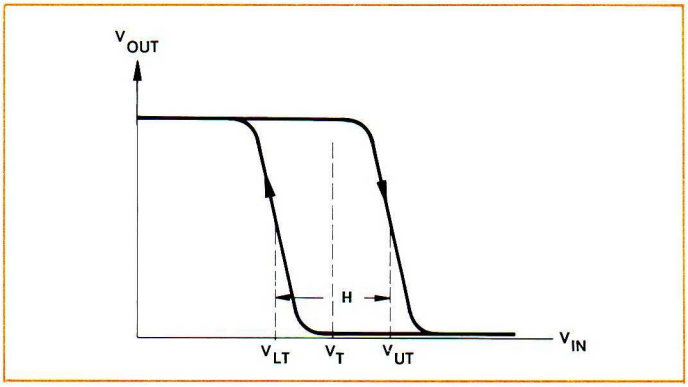


Fig. 4.101. Diagram transfer function

With the aid of CMOS NAND gates a Schmitt trigger with variable hysteresis can be designed.

The variable hysteresis is obtained because the MOS circuits can provide other output values than the logical "1" or "0". The inputs of a NAND gate can be fed with two different voltages and will then provide a varying output voltage depending on the combinations at the inputs, see fig. 4.102.

The output voltage is passing the transition level $V_{DD}/2$ for different values of V_{in}. The output can be set to trigger a flip-flop at a certain preset level ov V_{in}.

If V_{DD}, for example, is 10 V, the hysteresis range can vary between 5 V and about 9 V, i.e. approximately 40% of V_{DD} at a maximum.

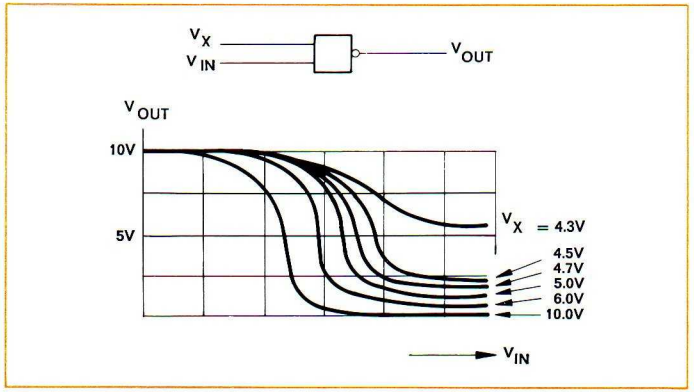


Fig. 4.102.

Exercise 31

Equipment required:

1 pulse generator PM 5705
1 oscilloscope PM 3232
1 DC power supply +10 V
1 CMOS circuit CD 4011A with datasheet
1 resistor 6.8 kohm
1 resistor 1 kohm
1 variable resistor 10 kohm
1 capacitor 0.1 μF

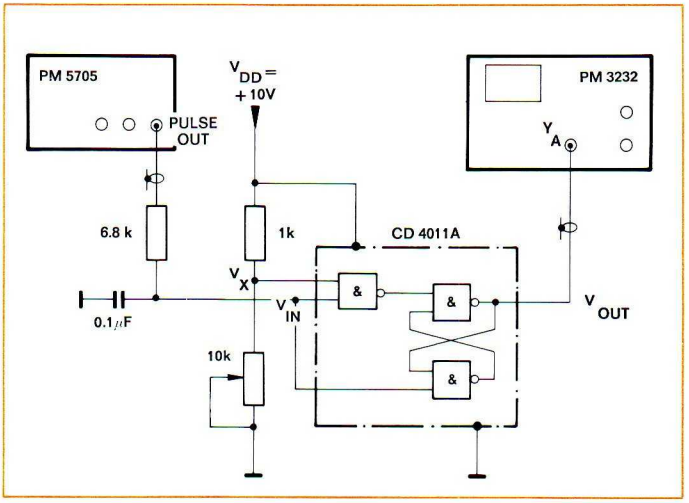


Fig. 4.103. Test set-up

The RC network connected to the pulse generator output provides a pulse with slow edges. The voltage divider 1 kohm and 10 kohm sets V_x between 0 V and approx. 10 V.

Set the pulse generator:		Set the oscilloscope:	
REP.TIME	6 ms	TIME/cm	400 μs
DURATION	1 ms	AMPL. A	5 V/cm
AMPL.	8 V		

WARNING!

The amplitude of the pulse generator may not exceed the supply voltage V_{DD} Otherwise the CMOS circuit may be damaged.

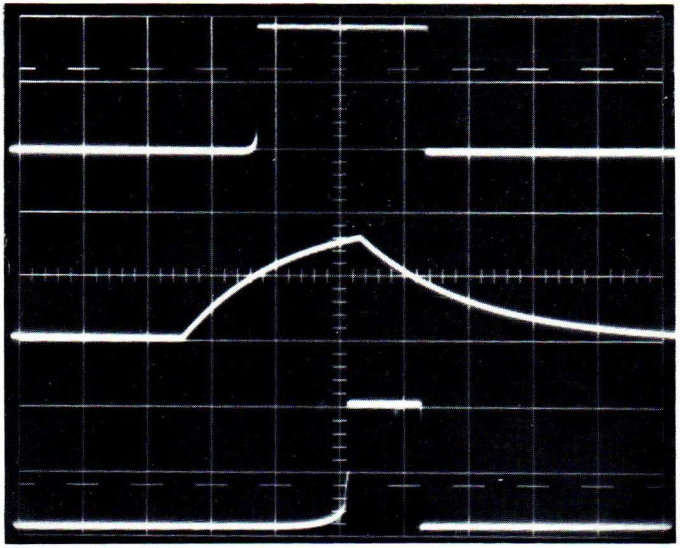


Fig. 4.104.

Upper trace: *output voltage V_{out} minimum hysteresis $V_x = 6.5$ V*
Middle trace: *input voltage V_{in}*
Lower trace: *output voltage V_{out} maximum hysteresis $V_x = 5$ V*

Fig. 4.104. shows a typical measurement result.

Note that the transition caused by the trailing edge of the input pulse always occurs at the same level because of the latch configuration formed by two of the NAND gates. Refer to exercise 14.

4. 20. Phase-lock circuit using CMOS Exclusive-OR gate

An Exclusive-OR gate has the following truth table

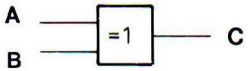


Fig. 4.105.

A	B	C
0	0	0
1	0	1
0	1	1
1	1	0

The CMOS package CD 4030A contains four dual-input Exclusive-OR gates. If such a gate is powered with V_{DD} 5 V it can be controlled by two different signals: one square wave signal from the TTL output (Normal or Complementary), and from the main pulse output, 4 V amplitude and variable duration.

Exercise 32

Preparatory verification of truth table for Exclusive-OR gate.

Equipment required:

1 pulse generator PM 5705
1 oscilloscope PM 3232
1 CMOS circuit CD 4030A with datasheet
1 DC power supply +5 V (PM 5704)

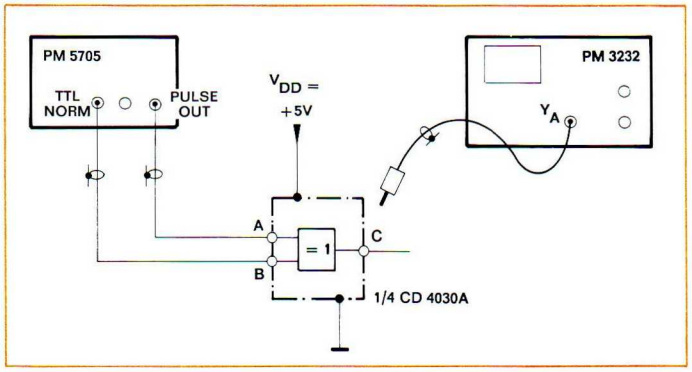


Fig. 4.106. Test set-up

WARNING!

The amplitude of the pulse generator may not exceed the supply voltage +5 V. Otherwise the CMOS circuit may be damaged.

Set the pulse generator:

REP.TIME 400 μs
DURATION 100 μs ... (variable)
SQUARE WAVE
NORMAL
AMPL. 4 V

Set the oscilloscope:

TIME/cm 50 μs
AMPL. A 2 V/cm

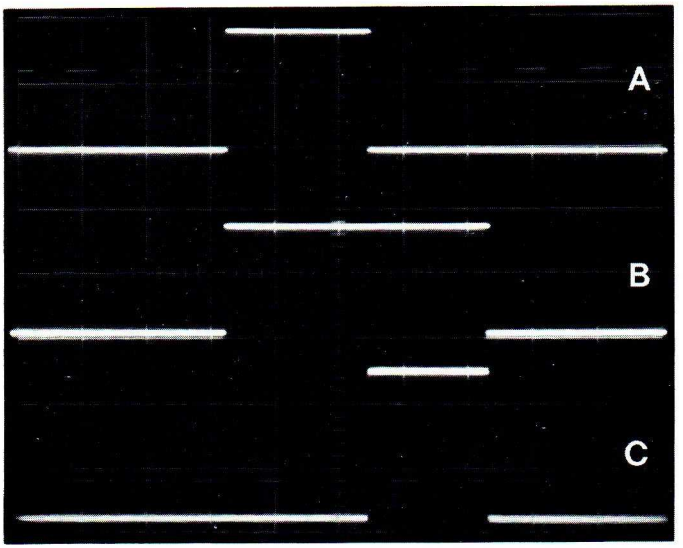


Fig. 4.107.

A. Main pulse from pulse generator
B. TTL pulse from pulse generator
C. Output pulse from the Excl. OR gate

Fig. 4.107. shows a typical measurement result.

The Exclusive-OR gate is used in phase-locked loops (PLL) in which one wants to synchronize two different signals to each other, e.g. two signal generators.

If the frequency of one of the signal generators can be controlled by an external voltage, this voltage can be taken from the Exclusive-OR gate via a low-pass filter which provides the mean value of the difference signal obtained from the gate.

Exercise 33

The phase-locking principle can be illustrated with the PM 5705 using the same technique as in exercise 32.

Use the same equipment, but add:

1 resistor 22 kohm
1 capacitor 0.68 μF
1 voltmeter

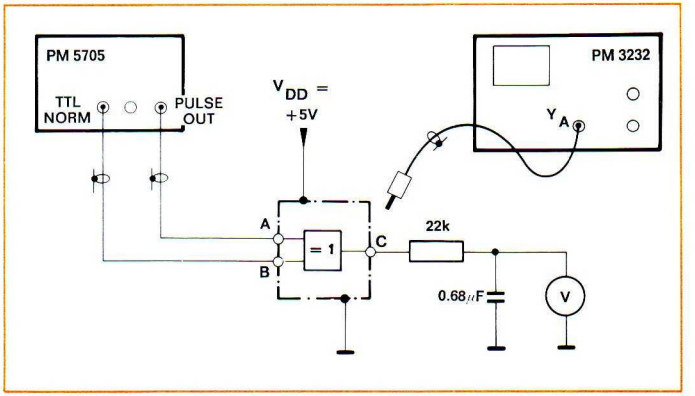


Fig. 4.108. Test set-up

Set the pulse generator:

REP.TIME 600 μs
DURATION 300 μs
AMPL. 4 V
SQUARE WAVE
NORMAL

Set the oscilloscope:

TIME/cm 50 μs
AMPL. A 2 V/cm

WARNING!

The amplitude of the pulse generator may not exceed the supply voltage +5 V. Otherwise the CMOS circuit may be damaged.

First case (fig. 4.109.)

Note that the input signals are almost in phase which makes that the Exclusive-OR gate provides very short pulses. This implies a very small correction of the frequency.
The voltmeter shows virtually no voltage (V = 0).

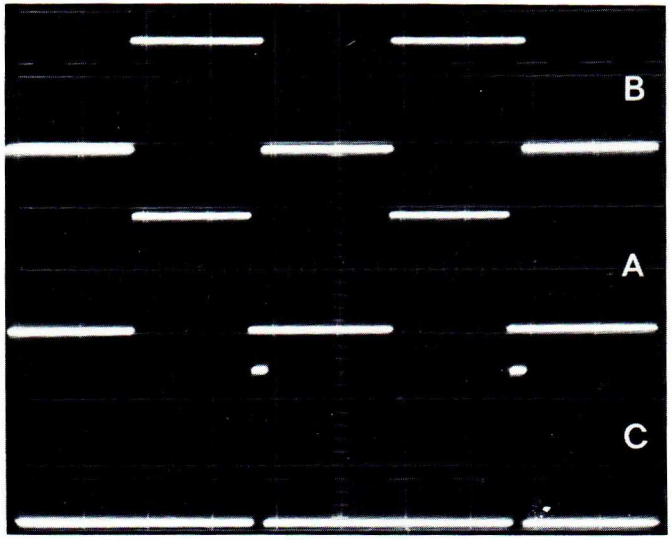


Fig. 4.109. *B. TTL pulse from pulse generator*
A. Main pulse from pulse generator
C. Output signal from the Exclusive-OR gate

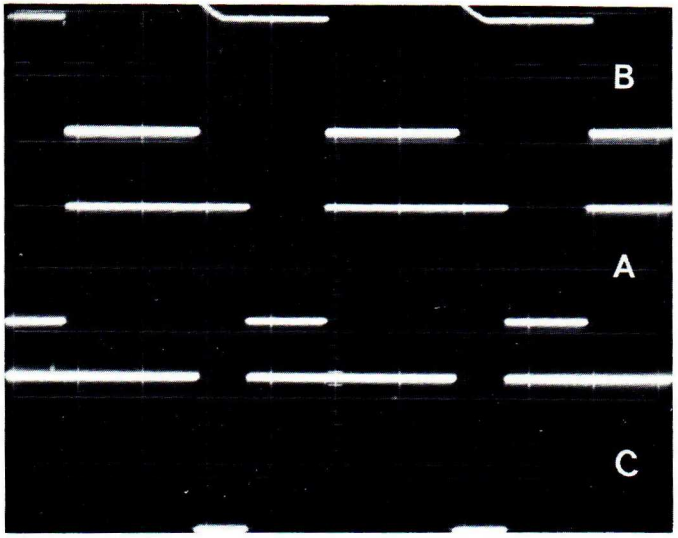


Fig. 4.110. *B. TTL pulse COMPL from pulse generator*
A. Main pulse from pulse generator
C. Output signal from the Exclusive-OR gate

Second case (fig. 4.110.)
The input signals are about 50% out of phase. The Exclusive-OR gate (C) provides a pulse train with duty factor 0.5 which implies a correction of the frequency. $V = 0.5 \times V_{max}$.

Third case (fig. 4.111.)
The input signals are almost completely out of phase. The Exclusive-OR gate provides a high level which implies a correction of the frequency. $V = V_{max}$

In the diagram fig. 4.112. a practical set-up is outlined.

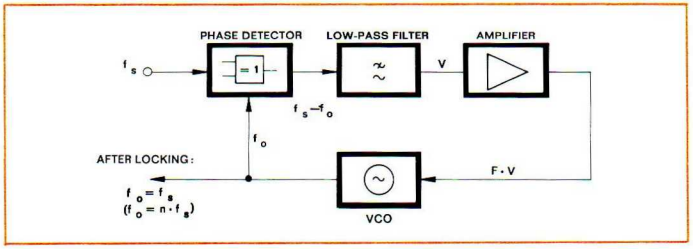


Fig. 4.112.

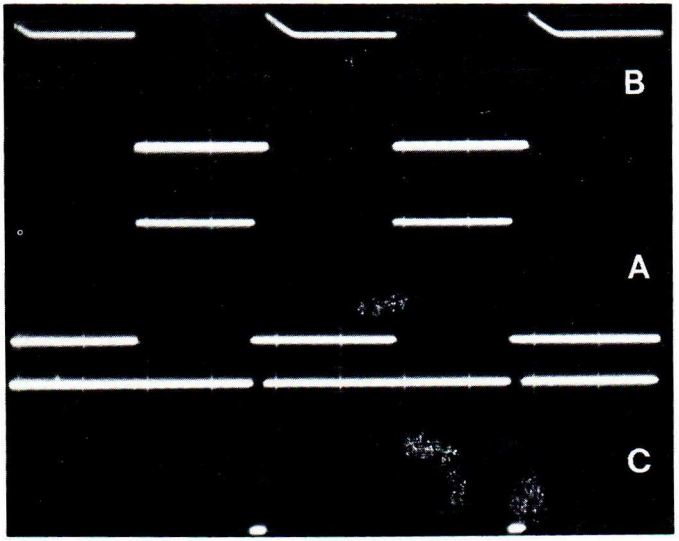


Fig. 4.111. *B. TTL pulse COMPL from pulse generator*
A. Main pulse from pulse generator
C. Output signal from the Exclusive-OR gate

4. 21. Reducing the power consumption of a LED display

1. Light sensitivity and inertia of the human eye

To extend the lifetime of the batteries in pocket calculators and similar battery powered apparatuses, the digital display can be fed with pulses instead of a dc voltage. Such an approach will reduce the power consumption considerably.

The requirements, however, are that the intensity of light is sufficient and that the light is constant without flicker. To this end the inertia of the human eye is utilized. The eye acts namely as an oscilloscope having a very fast risetime and a considerably slower fall time. This means that a light spot is registered on the retina in a very short time and is maintained there a long time after that the light pulse actually has disappeared. This phenomenon can be investigated by means of a pulse generator and a light-emitting diode.

Exercise 34

Equipment required:

1 pulse generator PM 5705 (PM 5704)
1 d.c. power supply +5 V (can be replaced by PM 5704)
1 TTL circuit SN 7400 with datasheet
1 light-emitting diode
1 resistor 680 ohm
1 resistor 100 ohm

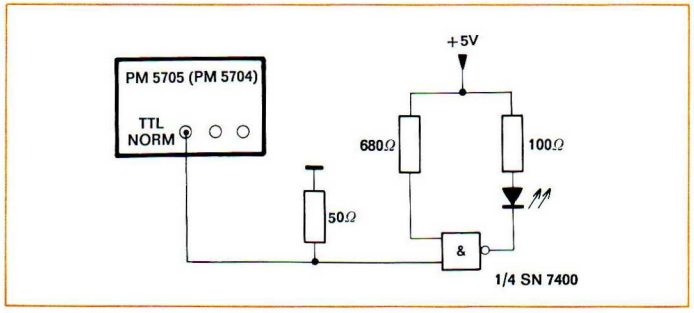


Fig. 4.113. Test set-up

The pulse amplitude is kept at a constant level because the light-emitting diode is fed with pulses from the NAND gate.

The shortest noticeable light pulse can now be measured by varying the pulse duration. Also the influence of the repetition frequency can be observed.

The shortest noticeable light pulse at decreasing repetition time is listed in the following table:

REP.TIME	DURATION
1 ms	< 50 ns
10 ms	≈ 150 ns
100 ms	≈ 500 ns
1 s	≈ 600 ns
10 s	≈ 600 ns

2. Power consumption of LED display

Exercise 35

Equipment required:

1 pulse generator PM 5705
1 d.c. power supply +5 V (PM 5704 can be used)
1 TTL circuit SN 7400 with datasheet
3 light-emitting diodes
2 resistors 680 ohm
3 resistors 100 ohm

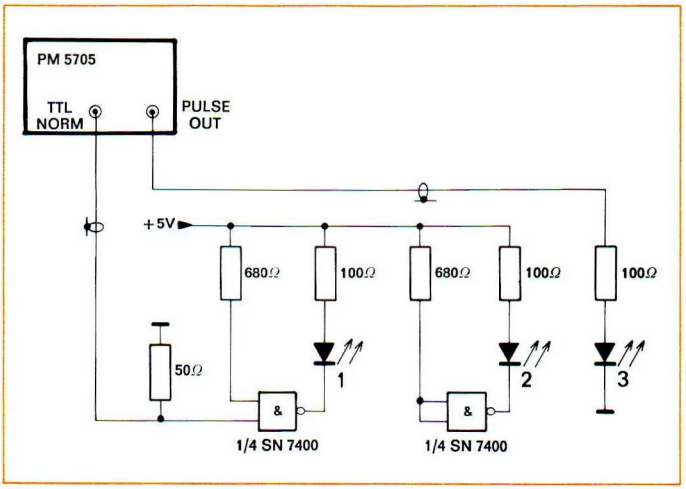


Fig. 4.114. Test set-up

Set the pulse generator:

AMPL. 15 V
NORMAL

Proceed as follows:

Adjust the pulse duration. Set the pulse generator until the light intensity of diode 1 (pulsed) approximately equals that of diode 2 (dc-powered).

Conclusion: An acceptable light intensity of diode 1 is achieved with duty factor 0.5 and independent of the pulse spacing as long as the flickering frequency is exceeded.

A duty factor of 0.5 ($\frac{\text{duration}}{\text{rep.time}} = 0{,}5$) gives an equivalent d.c. level of $\frac{E}{2}$ Volts. This means that the load, i.e. the diode, consumes 50% of the power needed at dc voltage supply.

If the amplitude of the pulses is increased, it can be seen that the voltage drop across the diode is constant ($V_D = 1.5$ V).

The diode power is $V_D \times I_P$, where I_P is the amplitude of the current pulse $(E—V_D)/R$. This current pulse can be replaced by an equivalent dc current

$$\bar{I}_P = I_P \times \frac{\text{Duration}}{\text{Rep.time}}$$

$V_D \times \bar{I}_P$ then corresponds to the average power in the diode which can be compared to the power at a dc supplied diode.

Set the pulse amplitude to 15 V and compare the light intensity of diode 2 with that of diode 3 at some different pulse duration and repetition time settings. Calculate the average power developed in the diode as a percentage of the power developed in a dc supplied diode.

Rep.time	Duration	Average power
10 ms	2 ms	77%
1 ms	0.2 ms	77%
100 μs	15 μs	58%
10 μs	1 μs	39%

5 List of exercises

1 Preparatory measurement of pulse parameters
2 Measuring the rise time of the main pulse of PM 5705
3 Measuring the fall time of the main pulse of PM 5705
4 Measuring the rise time of the TTL pulse of PM 5705 (PM 5704)
5 Measuring the fall time of the TTL pulse of PM 5705 (PM 5704)
6 Measuring the preshoot of a TTL pulse
7 TDR measurement
8 Measuring the influence of the cables on the waveform
9 Determining the recovery time of a power diode
10 Transients on the TTL supply voltage
11 Faults in a memory caused by interfering transients
12 Contact bounces
13 Contact bounces triggering a TTL circuit
14 Eliminating influence of contact bounces using RS flip-flop
15 Influence of pulse generator impedance on a TTL gate
16 Influence of pulse generator impedance on a decade counter
17 Delaying pulses I: hazard pulses
18 Delaying pulses II: known delay using RC network
19 Delaying pulses III: known delay using one-shots
20 Ripple 4-bit counter
21 Ripple decade counter
22 Modified ripple counter
23 Synchronous counter using JK flip-flops
24 Decade counter
25 CMOS power consumption
26 TTL power consumption
27 CMOS vs TTL: speed
28 CMOS vs TTL: supply voltage influence on rise time
29 CMOS risetime variation with changed supply voltage
30 CMOS analog amplifier
31 Measuring hysteresis of CMOS Schmitt trigger
32 Phaselock circuit using CMOS Exclusive-OR gate
33 Phaselock circuit using CMOS Exclusive-OR gate
34 Inertia of human eye: experiment with LED's
35 Reducing power consumption of a LED display.

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